

MultiGuard (2&4 Elements)

AVX Multilayer Ceramic Transient Voltage Suppression Arrays – ESD Protection for CMOS and Bi Polar Systems



GENERAL DESCRIPTION AND COMMENTS

AVX's Transient Voltage Suppression (TVS) Arrays address six trends in today's electronic circuits: (1) mandatory ESD protection, (2) mandatory EMI control, (3) signal integrity improvement, (4) PCB downsizing, (5) reduced component placement costs, and (6) protection from induced slow speed transient voltages and currents.

AVX's MultiGuard products offer numerous advantages, which include a faster turn-on-time (<1nS), repetitive strike capability, and space savings. In some cases, MultiGuard consumes less than 75% of the PCB real estate required for the equivalent number of discrete chips. This size advantage, coupled with the savings associated with placing only one chip, makes MultiGuard the TVS component of choice for

ESD protection of I/O lines in portable equipment and programming ports in cellular phones. Other applications include differential data line protection, ASIC protection and LCD driver protection for portable computing devices.

Where multiple lines require the ESD protection, the 4-element 0612 chip is an ideal solution. The 2-element 0405 MultiGuard is the smallest TVS array device available in the market today.

Available with standard working voltage of 5.6V up to 18V with low capacitance in the 3 case sizes, AVX MultiGuard arrays offer a very broad range of integrated TVS solutions to the design community.



ELECTRICAL CHARACTERISTICS PER ELEMENT

	AVX Part Number	Working Voltage (DC)	Working Voltage (AC)	Breakdown Voltage	Clamping Voltage	Test Current For V_c	Maximum Leakage Current	Transient Energy Rating	Peak Current Rating	Typical Cap
2 Element 0405 Chip	MG042S05X150 __	5.6	4.0	8.5±20%	18	1	35	0.05	15	300
	MG042L14V400 __	14.0	10.0	18.5±12%	32	1	15	0.02	15	45
	MG042L18V500 __	18.0	14.0	N/A	50	1	10	0.02	15	40
2 Element 0508 Chip	MG052S05A150 __	5.6	4.0	8.5±20%	18	1	35	0.10	30	825
	MG052S09A200 __	9.0	6.4	12.7±15%	22	1	25	0.10	30	550
	MG052S14A300 __	14.0	10.0	19.5±12%	32	1	15	0.10	30	425
	MG052S18A400 __	18.0	14.0	25.5±10%	42	1	10	0.10	30	225
	MG052L18X500 __	≤18.0	≤14.0	N/A	50	1	10	0.10	20	50
4 Element 0612 Chip	MG064S05A150 __	5.6	4.0	8.5±20%	18	1	35	0.10	30	825
	MG064S09A200 __	9.0	6.4	12.7±15%	22	1	25	0.10	30	550
	MG064S14A300 __	14.0	10.0	19.5±12%	32	1	15	0.10	30	425
	MG064S18A400 __	18.0	14.0	25.5±10%	42	1	10	0.05	15	120
	MG064L18X500 __	≤18.0	≤14.0	N/A	50	1	10	0.10	20	75

Termination Finish Code
Packaging Code

V_w (DC) DC Working Voltage (V)
 V_w (AC) AC Working Voltage (V)
 V_B Typical Breakdown Voltage (V @ 1mA_{DC})
 V_B Tol V_B Tolerance is ± from Typical Value

V_c Clamping Voltage (V @ I_c)
 I_c Test Current for V_c (A, 8x20μS)
 I_l Maximum Leakage Current at the Working Voltage (μA)
 E_T Transient Energy Rating (J, 10x1000μS)
 I_p Peak Current Rating (A, 8x20μS)
Cap Typical Capacitance (pF) @ 1MHz and 0.5 V_{RMS}

MultiGuard (2&4 Elements)

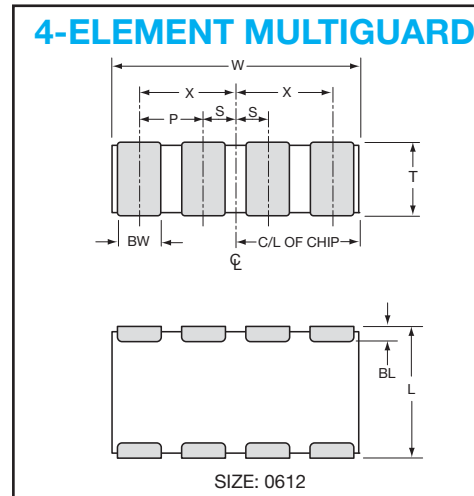
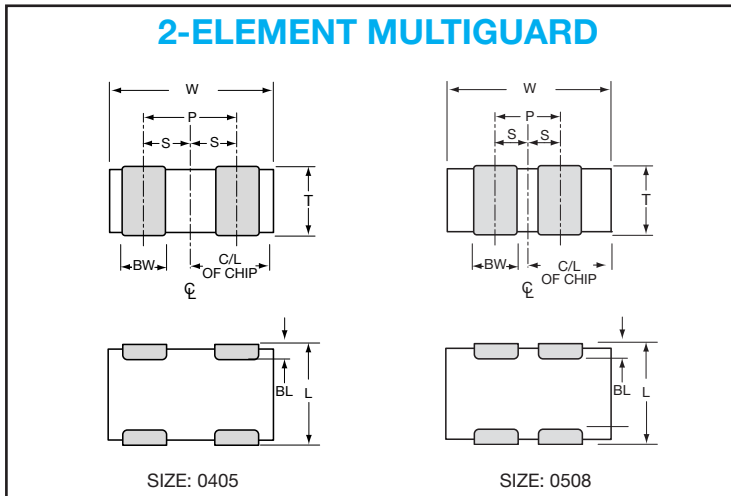


AVX Multilayer Ceramic

Transient Voltage Suppression Arrays

ESD Protection for CMOS and Bi Polar Systems

PHYSICAL DIMENSIONS AND PAD LAYOUT



0405 2 Element Dimensions mm (inches)

L	W	T	BW	BL	P	S
1.00±0.15 (0.039±0.006)	1.37±0.15 (0.054±0.006)	0.66 MAX (0.026 MAX)	0.36±0.10 (0.014±0.004)	0.20±0.10 (0.008±0.004)	064 REF (0.025 REF)	0.32±0.10 (0.013±0.004)

0612 4 Element Dimensions mm (inches)

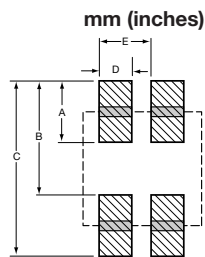
L	W	T	BW	BL	P	X	S
1.60±0.20 (0.063±0.008)	3.20±0.20 (0.126±0.008)	1.22 MAX (0.048 MAX)	0.41±0.10 (0.016±0.004)	0.18 ^{+0.25} _{-0.08} (0.007 ^{+0.10} _{-0.003})	0.76 REF (0.030 REF)	1.14±0.10 (0.045±0.004)	0.38±0.10 (0.015±0.004)

0508 2 Element Dimensions mm (inches)

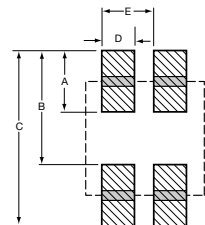
L	W	T	BW	BL	P	S
1.25±0.20 (0.049±0.008)	2.01±0.20 (0.079±0.008)	1.02 MAX (0.040 MAX)	0.41±0.1 (0.016±0.004)	0.18 ^{+0.25} _{-0.08} (0.007 ^{+0.10} _{-0.003})	0.76 REF (0.030 REF)	0.38±0.10 (0.015±0.004)

Pad Layout Dimensions

A	B	C	D	E
0405 2 Element				
0.46 (0.018)	0.74 (0.029)	1.20 (0.047)	0.38 (0.015)	0.64 (0.025)

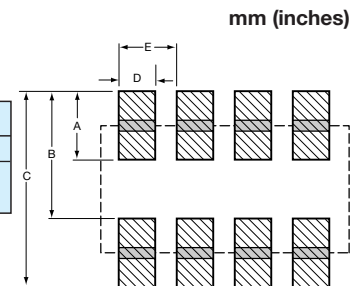


A	B	C	D	E
0508 2 Element				
0.89 (0.035)	1.27 (0.050)	2.16 (0.085)	0.46 (0.018)	0.76 (0.030)



Pad Layout Dimensions

A	B	C	D	E
0612 4 Element				
0.89 (0.035)	1.65 (0.065)	2.54 (0.100)	0.46 (0.018)	0.76 (0.030)



HOW TO ORDER

MG	04	2	L	14	A	300	T	P
MultiGuard	Case Size	Configuration	Style	Working Voltage	Energy Rating	Clamping Voltage	Packaging (PCS/REEL)	Termination Finish
	04 = 0405 05 = 0508 06 = 0612	2 = 2 Elements 4 = 4 Elements	S = Standard Construction L = Low Capacitance	05 = 5.6VDC 09 = 9.0VDC 14 = 14.0VDC 18 = 18.0VDC	A = 0.10 Joules V = 0.02 Joules X = 0.05 Joules	150 = 18V 200 = 22V 300 = 32V 400 = 42V 500 = 50V	D = 1,000 R = 4,000 T = 10,000	P = Ni/Sn Alloy (Plated) M = Ni/Sn Pb (Plated)



MultiGuard (2 & 4 Elements)

AVX Multilayer Ceramic

Transient Voltage Suppression Arrays

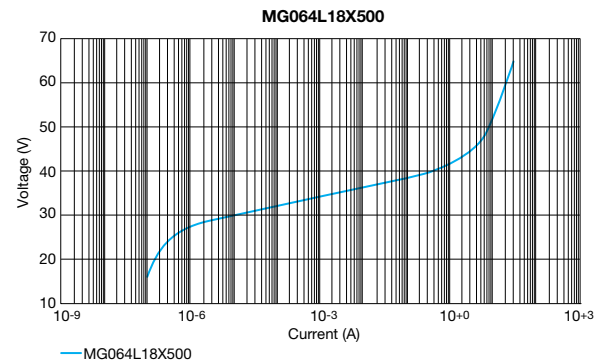
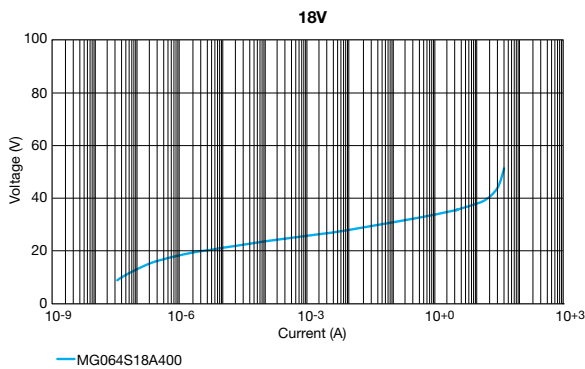
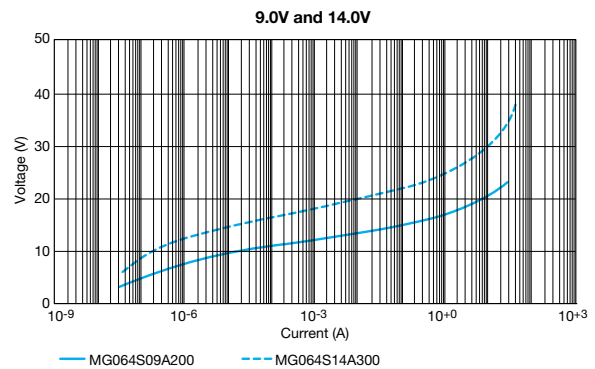
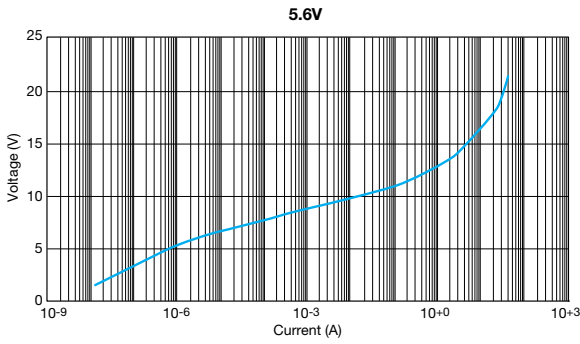
ESD Protection for CMOS and Bi Polar Systems



TYPICAL PERFORMANCE CURVES – VOLTAGE/CURRENT CHARACTERISTICS

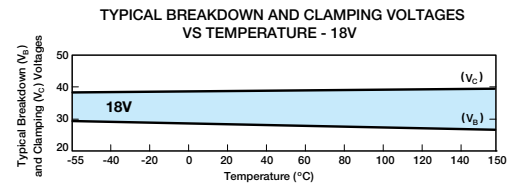
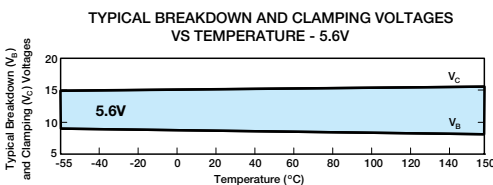
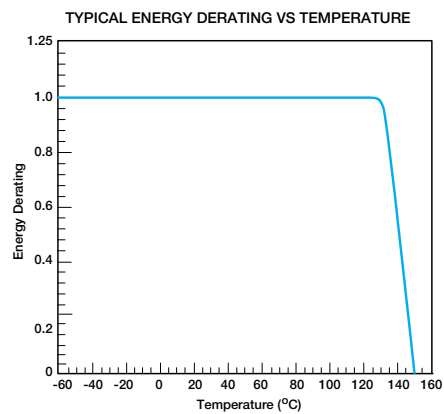
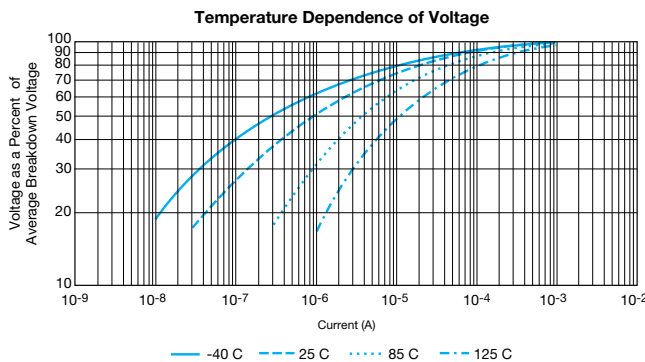
Multilayer construction and improved grain structure result in excellent transient clamping characteristics in excess of 30 amps (20 amps on MG064L18X500) peak current while maintaining very low leakage currents under DC operating

conditions. The VI curves below show the voltage/current characteristics for the 5.6V, 9V, 14V and 18V parts with currents ranging from fractions of a micro amp to tens of amps.



TYPICAL PERFORMANCE CURVES – TEMPERATURE CHARACTERISTICS

MultiGuard suppressors are designed to operate over the full temperature range from -55°C to +125°C.



MultiGuard (2 & 4 Elements)

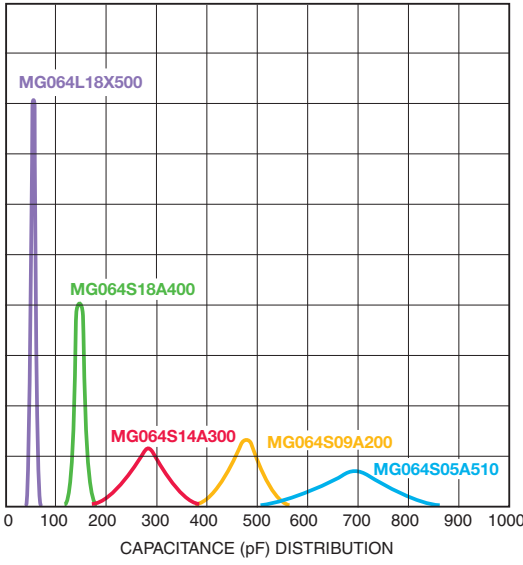
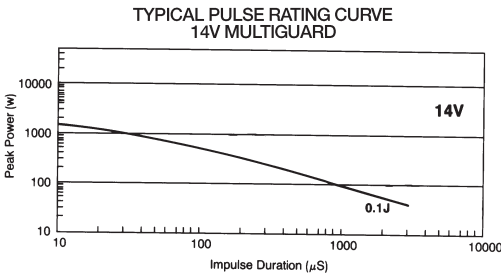
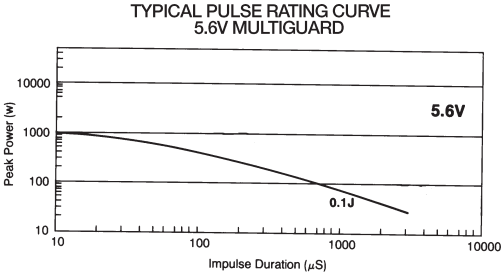
AVX Multilayer Ceramic

Transient Voltage Suppressors Arrays

ESD Protection for CMOS and Bi Polar Systems



TRANSIENT VOLTAGE SUPPRESSORS – TYPICAL PERFORMANCE CURVES



APPLICATION

