8-Channel Low Capacitance ESD Protection Arrays

Features

- 8 channels of ESD protection

  Note: For 2 and 4 channel devices, see the CM1293A datasheet.
- Provides ESD protection to IEC61000-4-2
  - ±8kV contact discharge
- Low loading capacitance of 2.0pF max.
- Low clamping voltage
- Channel I/O to I/O capacitance 1.5pF typical
- Zener diode protects supply rail and eliminates the need for external by-pass capacitors
- Each I/O pin can withstand over 1000 ESD strikes*
- Available in MSOP, lead-free packaging

Applications

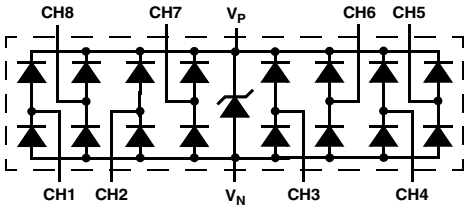
- DVI ports, HDMI ports in notebooks, set top boxes, digital TVs, LCD displays
- Serial ATA ports in desktop PCs and hard disk drives
- PCI Express ports
- General purpose high-speed data line ESD protection

Product Description

The CM1293 family of diode arrays has been designed to provide ESD protection for electronic components or sub-systems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. A Zener diode is embedded between V_P and V_N, offering two advantages. First, it protects the V_{CC} rail against ESD strikes, and second, it eliminates the need for a bypass capacitor that would otherwise be needed for absorbing positive ESD strikes to ground. The CM1293 will protect against ESD pulses up to (±8kV contact discharge) per the IEC 61000-4-2 Level 4 standard.

This device is particularly well-suited for protecting systems using high-speed ports such as USB2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

Electrical Schematic

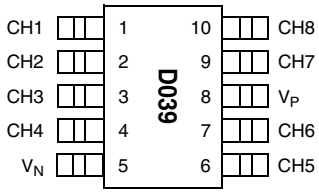


CM1293-08MR

*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to ±8kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

PACKAGE / PINOUT DIAGRAMS

Top View



10-Lead MSOP-10

Note: This drawing is not to scale.

PIN DESCRIPTIONS

8-CHANNEL, 10-LEAD MSOP-10 PACKAGE

PIN	NAME	TYPE	DESCRIPTION
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	CH3	I/O	ESD Channel
4	CH4	I/O	ESD Channel
5	V_N	PWR	Positive voltage supply rail
6	CH5	I/O	ESD Channel
7	CH6	I/O	ESD Channel
8	V_N	GND	Negative voltage supply rail
9	CH7	I/O	ESD Channel
10	CH8	I/O	ESD Channel

Ordering Information

PART NUMBERING INFORMATION				
			Lead-free Finish	
# of Channels	Leads	Package	Ordering Part Number[1]	Part Marking
8	10	MSOP-10	CM1293-08MR	D039

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
Operating Supply Voltage (V_P - V_N)	6.0	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	(V_N - 0.5) to (V_P + 0.5)	V

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Operating Temperature Range	-40 to +85	°C
Package Power Rating MSOP-10 Package (CM1293-08MR)	400	mW

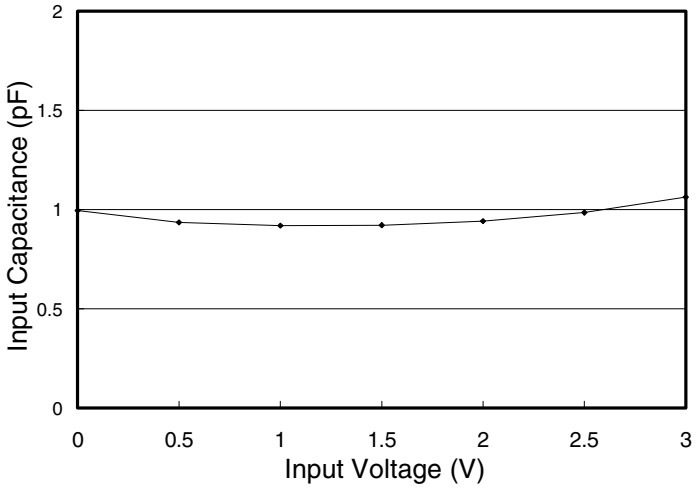
Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_P	Operating Supply Voltage (V_P-V_N)			3.3	5.5	V
I_P	Operating Supply Current	(V_P-V_N)=3.3V			8.0	µA
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8mA; T_A=25°C	 0.60 0.60	 0.80 0.80	 0.95 0.95	 V V
I_{LEAK}	Channel Leakage Current	T_A=25°C; V_P=5V, V_N=0V		±0.1	±1.0	µA
C_{IN}	Channel Input Capacitance	At 1 MHz, V_P=3.3V, V_N=0V, V_{IN}=1.65V; Note 2 applies		1.0	1.5	pF
ΔC_{IN}	Channel Input Capacitance Matching	At 1 MHz, V_P=3.3V, V_N=0V, V_{IN}=1.65V; Note 2 applies		0.02		pF
C_{MUTUAL}	Mutual Capacitance between signal pin and adjacent signal pin	At 1 MHz, V_P=3.3V, V_N=0V, V_{IN}=1.65V; Note 2 applies		0.11		pF
V_{ESD}	ESD Protection Peak Discharge Voltage at any channel input, in system Contact discharge per IEC 61000-4-2 standard	Notes 2, 4 & 5; T_A=25°C	±8			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	T_A=25°C, I_{PP} = 1A, t_P = 8/20uS; Notes 2, & 5		 +8.8 -1.4		 V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	I_{PP} = 1A, t_P = 8/20uS Any I/O pin to Ground; Note 2 and 5		 0.7 0.4		 Ω Ω

Note 1: All parameters specified at T_A = -40°C to +85°C unless otherwise noted.
Note 2: These parameters guaranteed by design and characterization.
Note 3: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5KΩ, V_P = 3.3V, V_N grounded.
Note 4: Standard IEC 61000-4-2 with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω, V_P = 3.3V, V_N grounded.
Note 5: These measurements performed with no external capacitor on V_P (V_P floating).

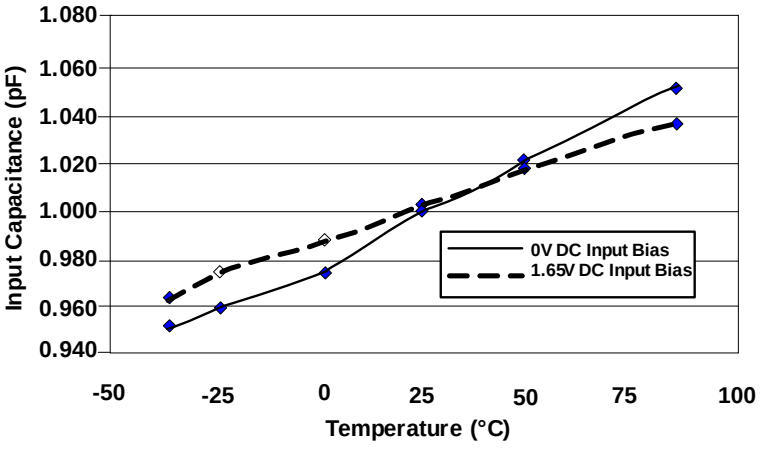
Performance Information

Input Channel Capacitance Performance Curves



Typical Variation of C_{IN} vs. V_{IN}

(f=1MHz, V_P = 3.3V, V_N = 0V, 0.1 µF chip capacitor between V_P and V_N, 25°C)



Typical Variation of C_{IN} vs. Temp

(f=1MHz, V_{IN}=30mV, V_P = 3.3V, V_N = 0V,
0.1 µF chip capacitor between V_P and V_N)

Performance Information (cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

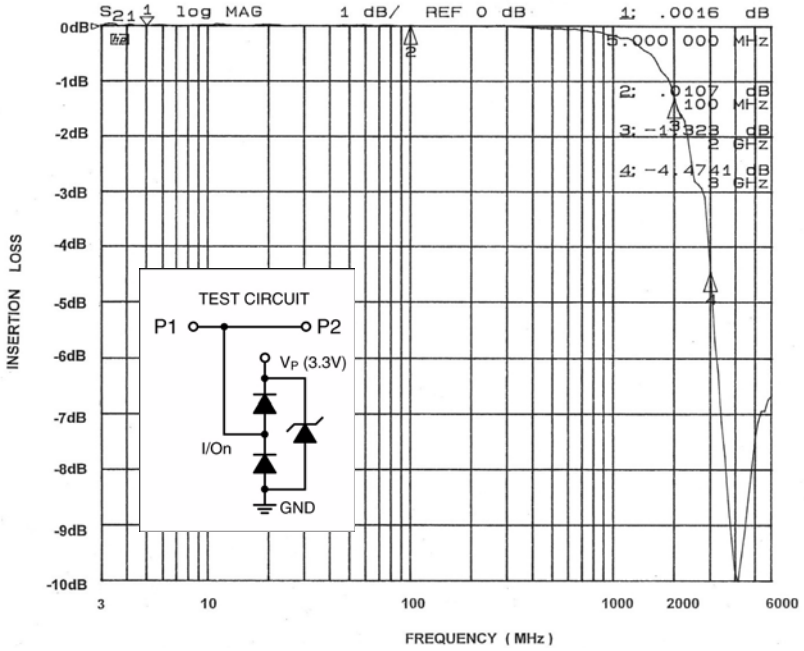


Figure 1. Insertion Loss (S21) VS. Frequency (0V DC Bias, V_P=3.3V)

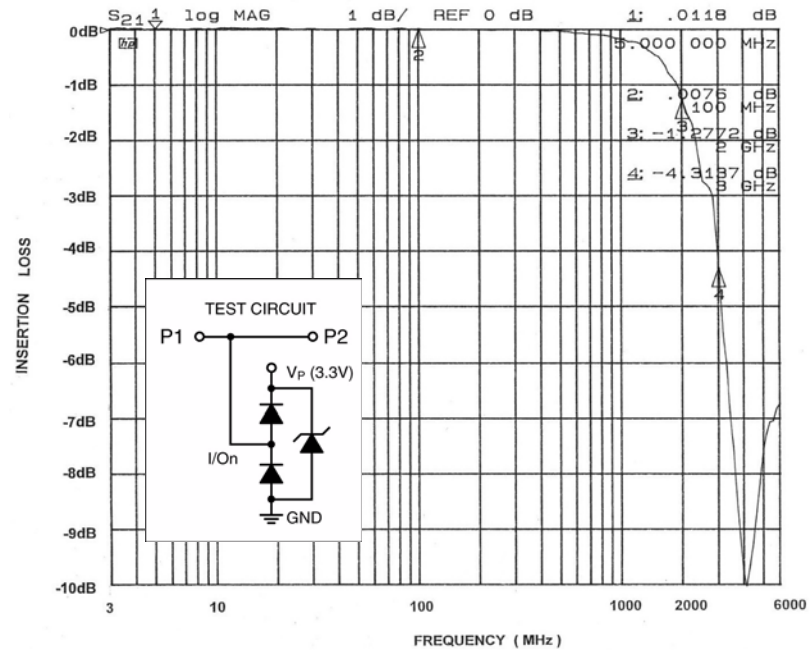


Figure 2. Insertion Loss (S21) VS. Frequency (2.5V DC Bias, V_P=3.3V)

Application Information

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/ Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Figure 3, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2. The voltage V_{CL} on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1ns. Here $d(I_{ESD})/dt$ can be approximated by $\Delta I_{ESD}/\Delta t$, or $30/(1x10^{-9})$. So just 10nH of series inductance (L_1 and L_2 combined) will lead to a 300V increment in V_{CL}!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1293 has an integrated Zener diode between V_P and V_N. This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the Zener diode. However, for the lowest possible V_{CL}, especially when V_P is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22µF ceramic chip capacitor be connected between V_P and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also California Micro Devices Application Note AP209, “Design Considerations for ESD Protection”, in the Applications section at www.calmicro.com.

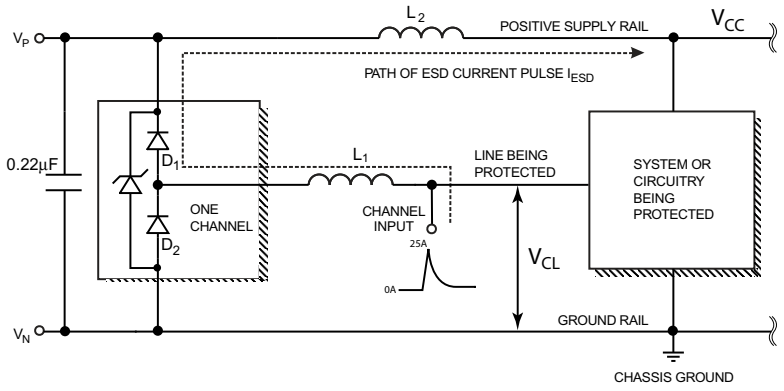


Figure 3. Application of Positive ESD Pulse between Input Channel and Ground

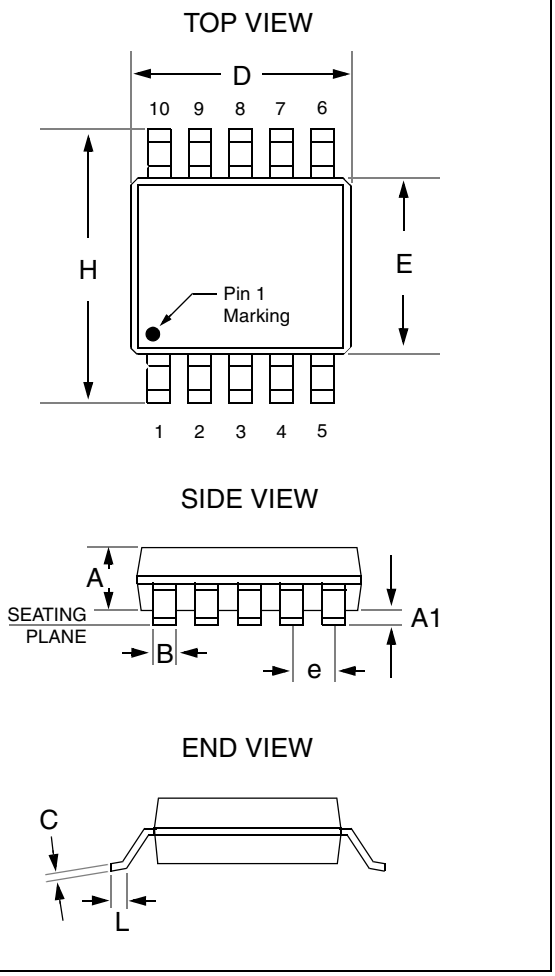
MS10 Mechanical Details

MSOP-10 Mechanical Specifications, 10 pin

The 10-pin MSOP package dimensions are presented below.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	10			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.75	0.95	0.028	0.038
A1	0.05	0.15	0.002	0.006
B	0.17	0.27	0.007	0.013
C	0.13	0.23	0.005	0.009
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.0196 BSC	
H	4.90 BSC		0.193 BSC	
L	0.40	0.70	0.0137	0.029
# per tape and reel	4000			
Controlling dimension: millimeters				

Mechanical Package Diagrams



Package Dimensions for MSOP-10