

FEATURES

- 14-bit resolution
- 8MHz guaranteed sampling rate
- No missing codes over full military temperature range
- Ideal for both time and frequency-domain applications
- Excellent THD (-75dB) and SNR (77dB)
- Edge-triggered; No pipeline delays
- Small, 24-pin, ceramic DDIP or SMT
- Requires only ±5V supplies
- Low-power, 2 Watts
- MIL-STD-883 screening optional



GENERAL DESCRIPTION

The low-cost ADS-946 is a 14-bit, 8MHz sampling A/D converter. This device accurately samples full-scale input signals up to Nyquist frequencies with no missing codes. Excellent differential nonlinearity error (DNL), signal-to-noise ratio (SNR), and total harmonic distortion (THD) make the ADS-946 the ideal choice for both time-domain (CCD/FPA imaging, scanners, process control) and frequency-domain (radar, telecommunications, spectrum analysis) applications.

The functionally complete ADS-946 contains a fast-settling sample-and-hold amplifier, a subranging (two-pass) A/D converter, an internal reference, timing/control logic, and error-correction circuitry. Digital input and output levels are TTL. The ADS-946 only requires the rising edge of a start convert pulse to operate.

Requiring only ±5V supplies, the ADS-946 typically dissipates just 2 Watts. The device is offered with a bipolar input range of ±2V. Models are available for use in either commercial (0 to +70°C) or military (-55 to +125°C) operating

INPUT/OUTPUT CONNECTIONS

| PIN | FUNCTION | PIN | FUNCTION |
|-----|-------------|-----|--------------------|
| 1 | BIT 1 (MSB) | 24 | ANALOG GROUND |
| 2 | BIT 2 | 23 | OFFSET ADJUST |
| 3 | BIT 3 | 22 | +5V ANALOG SUPPLY |
| 4 | BIT 4 | 21 | ANALOG INPUT |
| 5 | BIT 5 | 20 | -5V SUPPLY |
| 6 | BIT 6 | 19 | ANALOG GROUND |
| 7 | BIT 7 | 18 | START CONVERT |
| 8 | BIT 8 | 17 | EOC |
| 9 | BIT 9 | 16 | BIT 14 (LSB) |
| 10 | BIT 10 | 15 | BIT 13 |
| 11 | BIT 11 | 14 | DIGITAL GROUND |
| 12 | BIT 12 | 13 | +5V DIGITAL SUPPLY |

temperature ranges. A proprietary, auto-calibrating, error-correcting circuit allows the device to achieve specified performance over the full military temperature range.

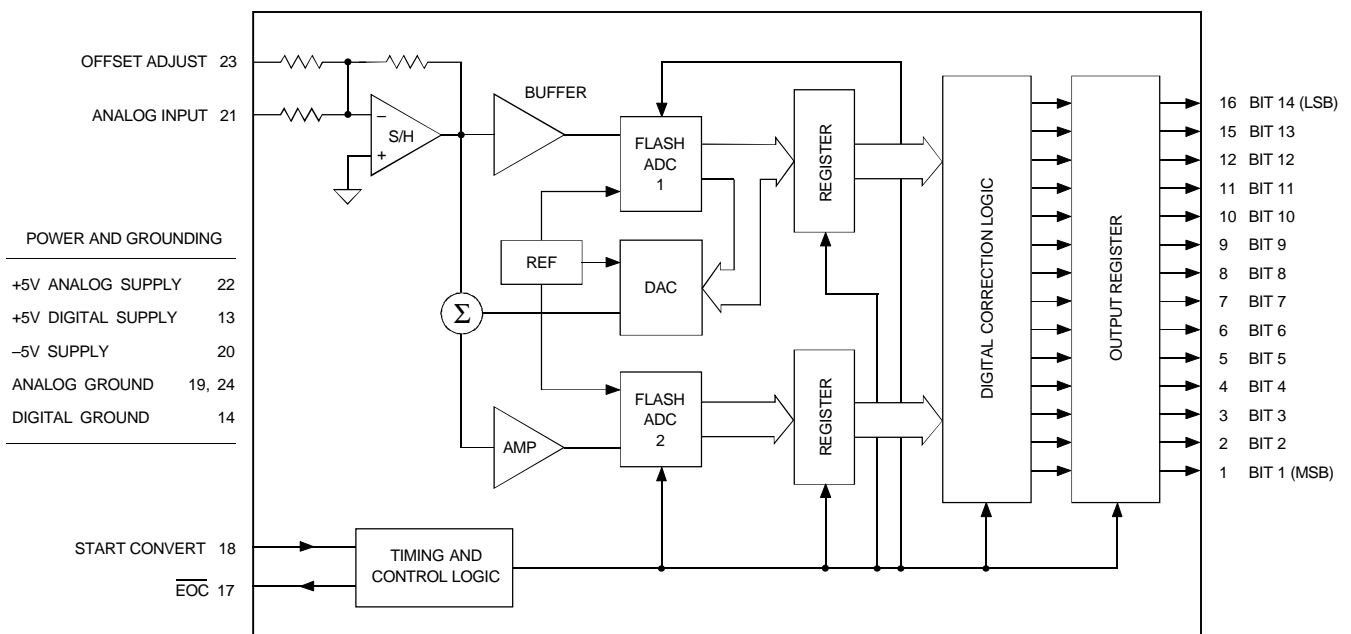


Figure 1. ADS-946 Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

| PARAMETERS | LIMITS | UNITS |
|-------------------------------|-------------------|-------|
| +5V Supply (Pins 13, 22) | 0 to +6 | Volts |
| -5V Supply (Pin 20) | 0 to -6 | Volts |
| Digital Input (Pin 18) | -0.3 to +VDD +0.3 | Volts |
| Analog Input (Pin 21) | ±5 | Volts |
| Lead Temperature (10 seconds) | +300 | °C |

PHYSICAL/ENVIRONMENTAL

| PARAMETERS | MIN. | TYP. | MAX. | UNITS |
|-----------------------------|---|------|------|---------|
| Operating Temp. Range, Case | 0 | — | +70 | °C |
| | -55 | — | +125 | °C |
| ADS-946MC, GC | | | | |
| ADS-946MM, GM, 883, G/883 | | | | |
| Thermal Impedance | — | 6 | — | °C/Watt |
| | — | 23 | — | °C/Watt |
| | — | — | — | °C |
| Storage Temperature Range | -65 | — | +150 | °C |
| Package Type | 24-pin, metal-sealed, ceramic DDIP or SMT | | | |
| Weight | 0.42 ounces (12 grams) | | | |

FUNCTIONAL SPECIFICATIONS

(TA = +25°C, ±VDD = ±5V, 8MHz sampling rate, and a minimum 3 minute warmup ① unless otherwise specified.)

| ANALOG INPUT | +25°C | | | 0 to +70°C | | | -55 to +125°C | | | UNITS |
|--|-------|-------|-------|------------|-------|-------|---------------|-------|-------|--------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| Input Voltage Range ② | — | ±2 | — | — | ±2 | — | — | ±2 | — | Volts |
| Input Resistance | — | 200 | — | — | 200 | — | — | 200 | — | Ω |
| Input Capacitance | — | 6 | 15 | — | 6 | 15 | — | 6 | 15 | pF |
| DIGITAL INPUT | | | | | | | | | | |
| Logic Levels | | | | | | | | | | |
| Logic "1" | +2.0 | — | — | +2.0 | — | — | +2.0 | — | — | Volts |
| Logic "0" | — | — | +0.8 | — | — | +0.8 | — | — | +0.8 | Volts |
| Logic Loading "1" | — | — | +20 | — | — | +20 | — | — | +20 | μA |
| Logic Loading "0" | — | — | -20 | — | — | -20 | — | — | -20 | μA |
| Start Convert Positive Pulse Width ③ | 10 | 20 | — | 10 | 20 | — | 10 | 20 | — | ns |
| STATIC PERFORMANCE | | | | | | | | | | |
| Resolution | — | 14 | — | — | 14 | — | — | 14 | — | Bits |
| Integral Nonlinearity (fin = 10kHz) | — | ±0.75 | — | — | ±0.75 | — | — | ±1 | — | LSB |
| Differential Nonlinearity (fin = 10kHz) | -0.95 | ±0.5 | +1.25 | -0.95 | ±0.5 | +1.25 | -0.95 | ±0.75 | +1.99 | LSB |
| Full Scale Absolute Accuracy | — | ±0.15 | ±0.4 | — | ±0.15 | ±0.4 | — | ±0.4 | ±0.8 | %FSR |
| Bipolar Zero Error (Tech Note 2) | — | ±0.2 | ±0.4 | — | ±0.2 | ±0.4 | — | ±0.4 | ±0.65 | %FSR |
| Gain Error (Tech Note 2) | — | ±0.2 | ±0.75 | — | ±0.2 | ±0.75 | — | ±0.4 | ±1.25 | % |
| No Missing Codes (fin = 10kHz) | 14 | — | — | 14 | — | — | 14 | — | — | Bits |
| DYNAMIC PERFORMANCE | | | | | | | | | | |
| Peak Harmonics (-0.5dB) | | | | | | | | | | |
| dc to 500kHz | — | -76 | -72 | — | -76 | -72 | — | -74 | -70 | dB |
| 500kHz to 1MHz | — | -75 | -72 | — | -75 | -72 | — | -74 | -68 | dB |
| 1MHz to 4MHz | — | -75 | -71 | — | -75 | -71 | — | -69 | -65 | dB |
| Total Harmonic Distortion (-0.5dB) | | | | | | | | | | |
| dc to 500kHz | — | -75 | -71 | — | -75 | -71 | — | -74 | -70 | dB |
| 500kHz to 1MHz | — | -75 | -70 | — | -75 | -70 | — | -72 | -68 | dB |
| 1MHz to 4MHz | — | -75 | -70 | — | -75 | -70 | — | -69 | -64 | dB |
| Signal-to-Noise Ratio (w/o distortion, -0.5dB) | | | | | | | | | | |
| dc to 500kHz | 73 | 77 | — | 73 | 77 | — | 72 | 76 | — | dB |
| 500kHz to 1MHz | 73 | 77 | — | 73 | 77 | — | 72 | 76 | — | dB |
| 1MHz to 4MHz | 73 | 77 | — | 73 | 77 | — | 72 | 76 | — | dB |
| Signal-to-Noise Ratio ④ (& distortion, -0.5dB) | | | | | | | | | | |
| dc to 500kHz | 70 | 74 | — | 70 | 74 | — | 68 | 73 | — | dB |
| 500kHz to 1MHz | 69 | 73 | — | 69 | 73 | — | 65 | 70 | — | dB |
| 1MHz to 4MHz | 69 | 73 | — | 69 | 73 | — | 65 | 70 | — | dB |
| Noise | — | 150 | — | — | 150 | — | — | 150 | — | μVrms |
| Two-Tone Intermodulation Distortion (fin = 2.45MHz, 1.975MHz, fs = 8MHz, -0.5dB) | — | -82 | — | — | -82 | — | — | -82 | — | dB |
| Input Bandwidth (-3dB) | | | | | | | | | | |
| Small Signal (-20dB input) | — | 30 | — | — | 30 | — | — | 30 | — | MHz |
| Large Signal (-0.5dB input) | — | 10 | — | — | 10 | — | — | 10 | — | MHz |
| Feedthrough Rejection (fin = 4MHz) | — | 85 | — | — | 85 | — | — | 85 | — | dB |
| Slew Rate | — | ±400 | — | — | ±400 | — | — | ±400 | — | V/μs |
| Aperture Delay Time | — | +5 | — | — | +5 | — | — | +5 | — | ns |
| Aperture Uncertainty | — | 2 | — | — | 2 | — | — | 2 | — | ps rms |

| DYNAMIC PERFORMANCE (Cont.) | +25°C | | | 0 to +70°C | | | -55 to +125°C | | | UNITS |
|--|---------------|------|-------|------------|------|---|---------------|------|-------|---------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| S/H Acquisition Time (to ±0.003%FSR, 4V step) | — | 55 | 60 | — | 55 | 60 | — | 55 | 60 | ns |
| Overvoltage Recovery Time ⑤ | — | 100 | 125 | — | 100 | 125 | — | 100 | 125 | ns |
| A/D Conversion Rate | 8 | — | — | 8 | — | — | 8 | — | — | MHz |
| DIGITAL OUTPUTS | | | | | | | | | | |
| Logic Levels | | | | | | | | | | |
| Logic "1" | +2.4 | — | — | +2.4 | — | — | +2.4 | — | — | Volts |
| Logic "0" | — | — | +0.4 | — | — | +0.4 | — | — | +0.4 | Volts |
| Logic Loading "1" | — | — | -4 | — | — | -4 | — | — | -4 | mA |
| Logic Loading "0" | — | — | +4 | — | — | +4 | — | — | +4 | mA |
| Output Coding | Offset Binary | | | | | | | | | |
| POWER REQUIREMENTS | | | | | | | | | | |
| Power Supply Ranges ⑥ | | | | | | | | | | |
| +5V Supply | +4.75 | +5.0 | +5.25 | +4.75 | +5.0 | +5.25 | +4.9 | +5.0 | +5.25 | Volts |
| -5V Supply | -4.75 | -5.0 | -5.25 | -4.75 | -5.0 | -5.25 | -4.9 | -5.0 | -5.25 | Volts |
| Power Supply Currents | | | | | | | | | | |
| +5V Supply | — | +250 | +270 | — | +250 | +270 | — | +250 | +270 | mA |
| -5V Supply | — | -150 | -170 | — | -150 | -170 | — | -150 | -170 | mA |
| Power Dissipation | — | 2 | 2.2 | — | 2 | 2.2 | — | 2 | 2.2 | Watts |
| Power Supply Rejection | — | — | ±0.05 | — | — | ±0.05 | — | — | ±0.05 | %FSR/%V |
| Footnotes: | | | | | | | | | | |
| ① All power supplies should be on before applying a start convert pulse. All supplies and the clock (start convert pulses) must be present during warmup periods. The device must be continuously converting during this time. | | | | | | ④ Effective bits is equal to: $\frac{(\text{SNR} + \text{Distortion}) - 1.76 + \left[20 \log \frac{\text{Full Scale Amplitude}}{\text{Actual Input Amplitude}} \right]}{6.02}$ | | | | |
| ② Contact DATEL for other input voltage ranges. | | | | | | ⑤ This is the time required before the A/D output data is valid once the analog input is back within the specified range. This time is only guaranteed if the input does not exceed ±2.2V (S/H saturation voltage). | | | | |
| ③ An 8MHz clock with a 20nsec positive pulse width is used for all production testing. See Timing Diagram, Figure 4, for more details. | | | | | | ⑥ The minimum supply voltages of +4.9V and -4.9V for ±VDD are required for -55°C operation only. The minimum limits are +4.75V and -4.75V when operating at +125°C | | | | |

TECHNICAL NOTES

1. Obtaining fully specified performance from the ADS-946 requires careful attention to pc card layout and power supply decoupling. The device's analog and digital ground systems are connected to each other internally. For optimal performance, tie all ground pins (14, 19 and 24) directly to a large *analog* ground plane beneath the package.

Bypass all power supplies to ground with 4.7µF tantalum capacitors in parallel with 0.1µF ceramic capacitors. Locate the bypass capacitors as close to the unit as possible.

2. The ADS-946 achieves its specified accuracies without the need for external calibration. If required, the device's small initial offset and gain errors can be reduced to zero using the adjustment circuitry shown in Figures 2 and 3. When using this circuitry, or any similar offset and gain calibration hardware, make adjustments following warmup. To avoid interaction, always adjust offset before gain.

- 3. Applying a start convert pulse while a conversion is in progress (EOC = logic 1) will initiate a new and inaccurate conversion cycle. Data for the interrupted and subsequent conversions will be invalid.
- 4. A passive bandpass filter is used at the input of the A/D for all production testing.

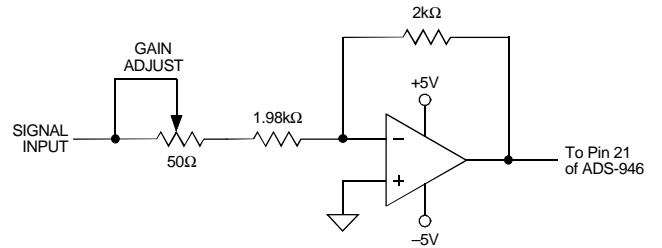


Figure 2. Optional ADS-946 Gain Adjust Calibration Circuit

CALIBRATION PROCEDURE

Any offset and/or gain calibration procedures should not be implemented until devices are fully warmed up. To avoid interaction, offset must be adjusted before gain. The ranges of adjustment for the circuits in Figures 2 and 3 are guaranteed to compensate for the ADS-946's initial accuracy errors and may not be able to compensate for additional system errors.

A/D converters are calibrated by positioning their digital outputs exactly on the transition point between two adjacent digital output codes. This can be accomplished by connecting LED's to the digital outputs and adjusting until certain LED's "flicker" equally between on and off. Other approaches employ digital comparators or microcontrollers to detect when the outputs change from one code to the next.

Offset adjusting for the ADS-946 is normally accomplished at the point where the MSB is a 1 and all other output bits are 0's and the LSB just changes from a 0 to a 1. This digital output transition ideally occurs when the applied analog input is $+1/2$ LSB (+122 μ V).

Gain adjusting is accomplished when all bits are 1's and the LSB just changes from a 1 to a 0. This transition ideally occurs when the analog input is at +full scale minus $1/2$ LSB's (+1.99963V).

Zero/Offset Adjust Procedure

1. Apply a train of pulses to the START CONVERT input (pin 18) so the converter is continuously converting.
2. Apply +122 μ V to the ANALOG INPUT (pin 21).
3. Adjust the offset potentiometer until the output bits are 10 0000 0000 0000 and the LSB flickers between 0 and 1.

Gain Adjust Procedure

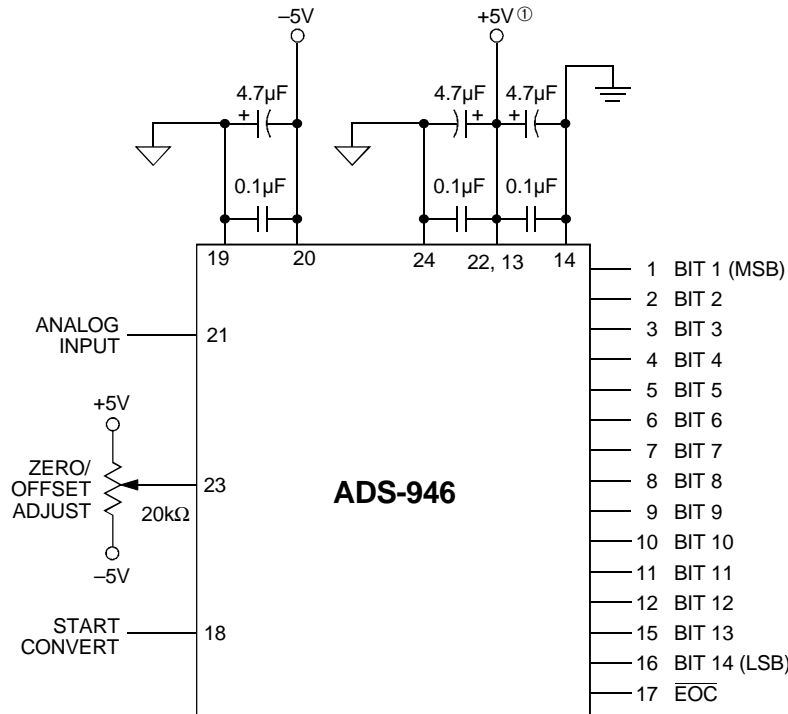
1. Apply +1.99963V to the ANALOG INPUT (pin 21).
2. Adjust the gain potentiometer until all output bits are 1's and the LSB flickers between 1 and 0.
3. To confirm proper operation of the device, vary the input signal to obtain the output coding listed in Table 2.

Table 1. Gain and Zero Adjust

| INPUT VOLTAGE RANGE | ZERO ADJUST $+1/2$ LSB | GAIN ADJUST $+FS -1/2$ LSB |
|---------------------|------------------------|----------------------------|
| $\pm 2V$ | +122 μ V | +1.99963V |

Table 2. Output Coding for Bipolar Operation

| BIPOLAR SCALE | INPUT VOLTAGE ($\pm 2V$ RANGE) | OFFSET BINARY MSB LSB |
|---------------|---------------------------------|-----------------------|
| +FS -1 LSB | +1.99976 | 11 1111 1111 1111 |
| +3/4 FS | +1.50000 | 11 1000 0000 0000 |
| +1/2 FS | +1.00000 | 11 0000 0000 0000 |
| 0 | 0.00000 | 10 0000 0000 0000 |
| -1/2 FS | -1.00000 | 01 0000 0000 0000 |
| -3/4 FS | -1.50000 | 00 1000 0000 0000 |
| -FS +1 LSB | -1.99976 | 00 0000 0000 0001 |
| -FS | -2.00000 | 00 0000 0000 0000 |



① A single +5V supply should be used for both the +5V analog and +5V digital. If separate supplies are used, the difference between the two cannot exceed 100mV.

Figure 3. Typical ADS-946 Connection Diagram

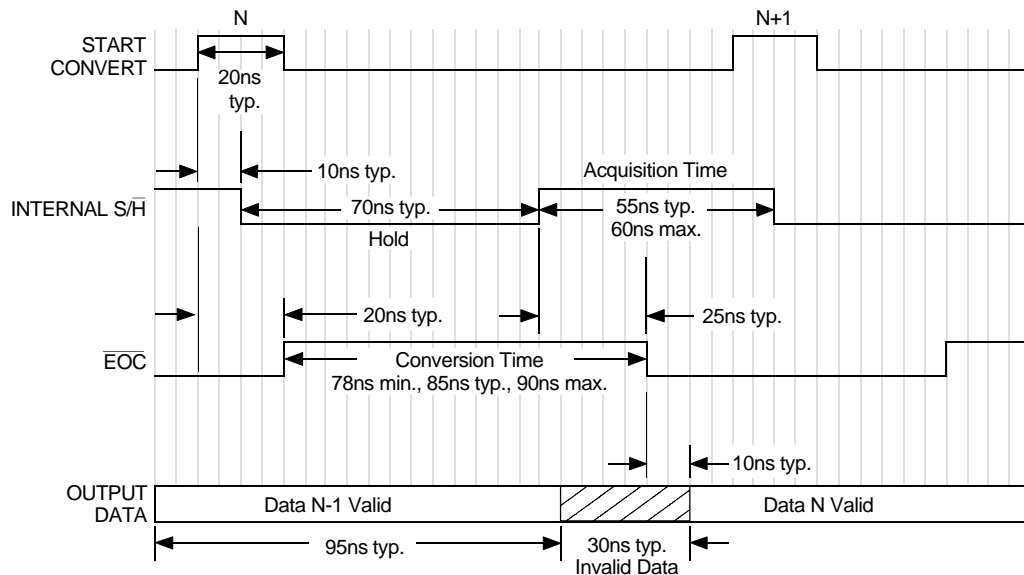
THERMAL REQUIREMENTS

All DATEL sampling A/D converters are fully characterized and specified over operating temperature (case) ranges of 0 to +70°C and -55 to +125°C. All room-temperature (TA = +25°C) production testing is performed without the use of heat sinks or forced-air cooling. Thermal impedance figures for each device are listed in their respective specification tables.

These devices do not normally require heat sinks, however, standard precautionary design and layout procedures should be used to ensure devices do not overheat. The ground and power planes beneath the package, as well as all pcb signal runs to and from the device, should be as heavy as possible to help conduct heat away from the package.

Electrically-insulating, thermally-conductive "pads" may be installed underneath the package. Devices should be soldered to boards rather than socketed, and of course, minimal air flow over the surface can greatly help reduce the package temperature.

In more severe ambient conditions, the package/junction temperature of a given device can be reduced dramatically (typically 35%) by using one of DATEL's HS Series heat sinks. See Ordering Information for the assigned part number. See page 1-183 of the DATEL Data Acquisition Components Catalog for more information on the HS Series. Request DATEL Application Note AN-8, "Heat Sinks for DIP Data Converters," or contact DATEL directly, for additional information.



Notes:

1. Scale is approximately 5ns per division. Sampling rate = 8MHz.
2. The start convert positive pulse width must be between 10 and 50ns or between 80 and 110ns (when sampling at 8MHz) to ensure proper operation. For sampling rates less than 8MHz, the start pulse can be wider than 110nsec, however a minimum pulse width low of 15nsec should be maintained. An 8MHz clock with a 20nsec positive pulse width is used for all production testing.

Figure 4. ADS-946 Timing Diagram

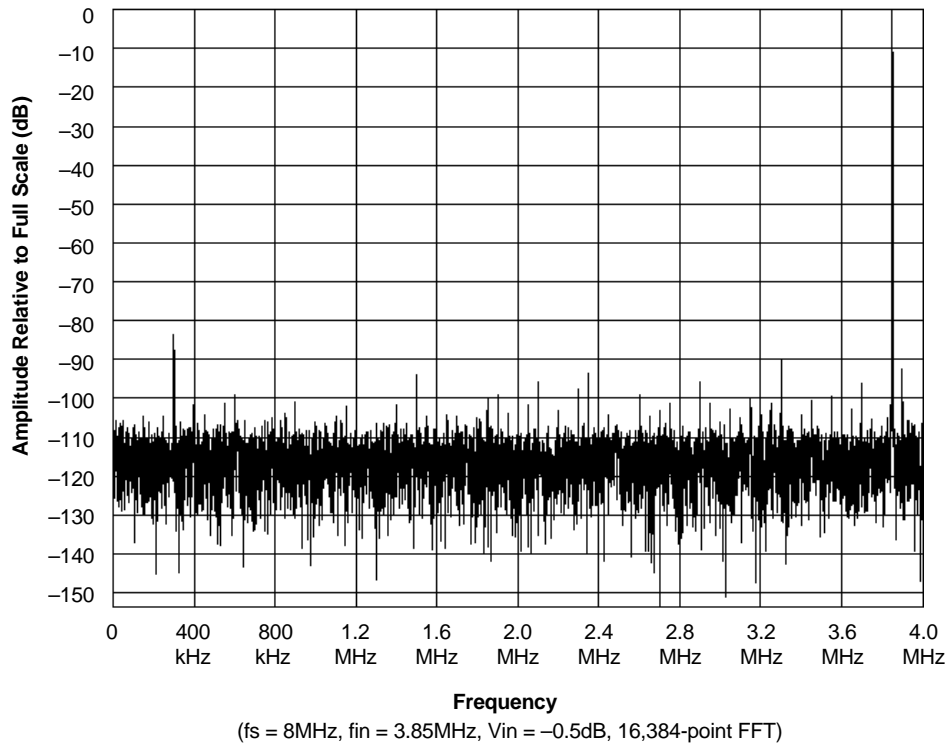


Figure 5. FFT Analysis of ADS-946

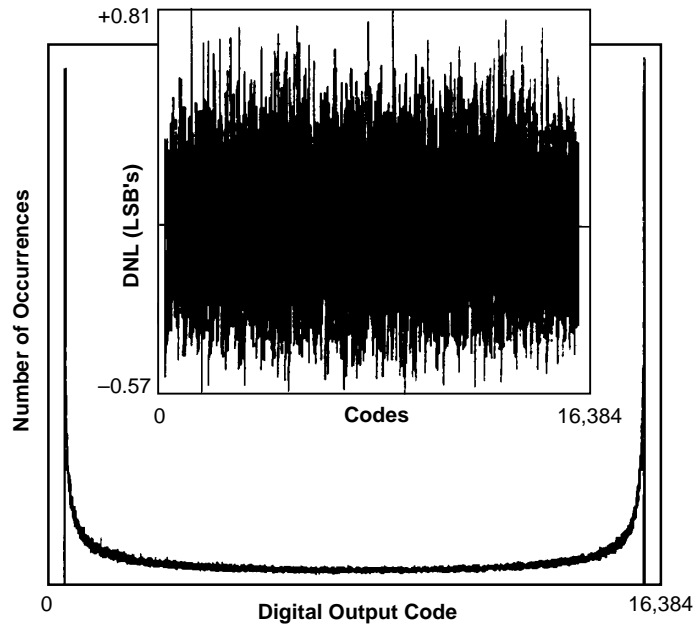
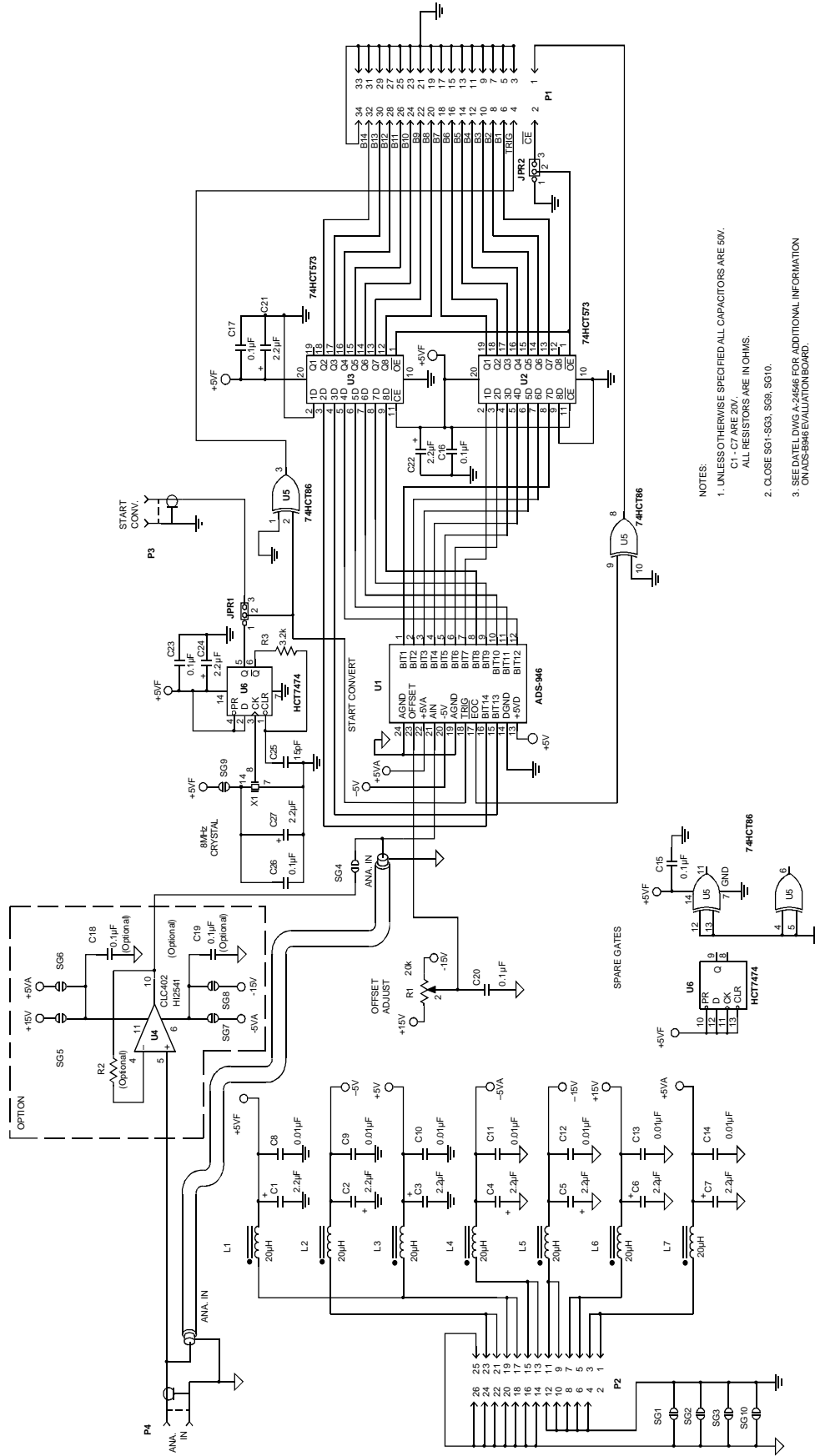


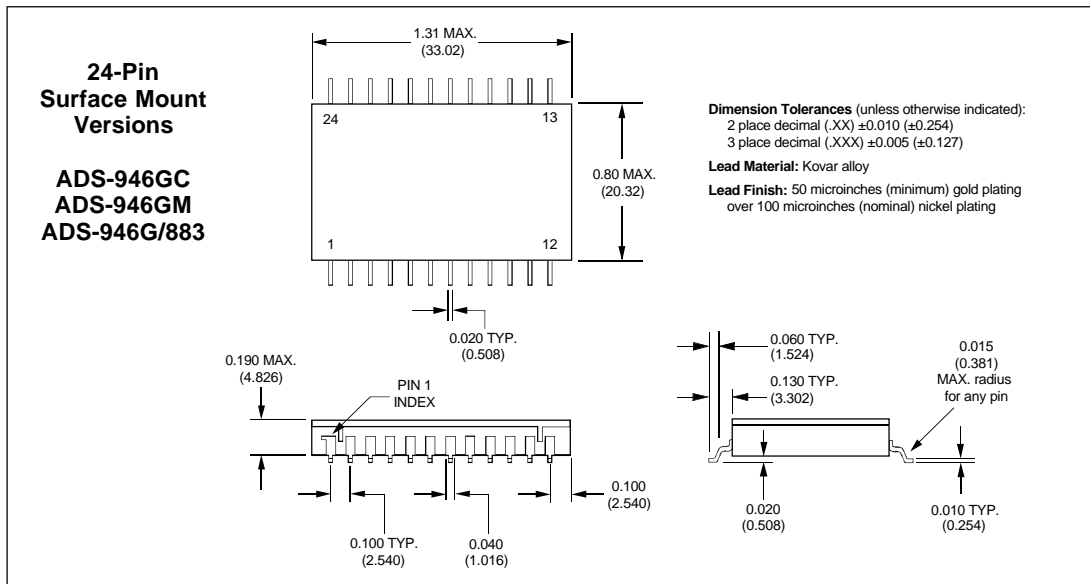
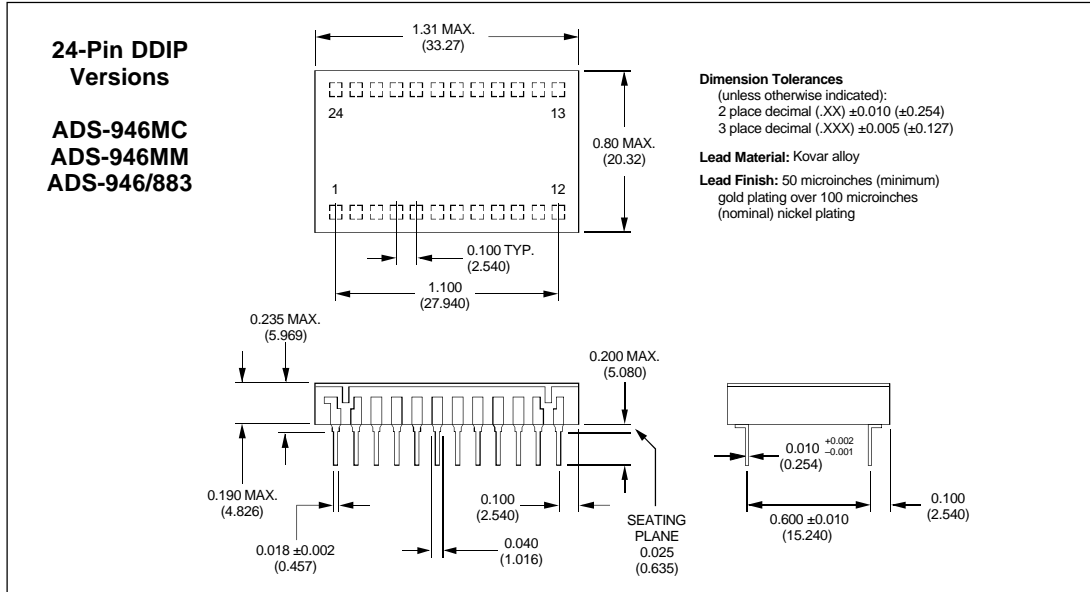
Figure 6. ADS-946 Histogram and Differential Nonlinearity



- NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL CAPACITORS ARE 50V. C1 - C7 ARE 20V. ALL RESISTORS ARE IN OHMS.
 2. CLOSE SG1-SG3, SG8, SG10.
 3. SEE DATTEL DYNASIS FOR ADDITIONAL INFORMATION ON ADS-B946 EVALUATION BOARD.

Figure 7. ADS-946 Evaluation Board Schematic (ADS-B946)

MECHANICAL DIMENSIONS INCHES (mm)



ORDERING INFORMATION

| MODEL | OPERATING TEMP. RANGE | 24-PIN PACKAGE | ACCESSORIES |
|--------------|-----------------------|----------------|--|
| ADS-946MC | 0 to +70°C | DDIP | ADS-B946 Evaluation Board (without ADS-946) HS-24 Heat Sink for all ADS-946 DDIP models |
| ADS-946MM | -55 to +125°C | DDIP | |
| ADS-946/883 | -55 to +125°C | DDIP | |
| ADS-946GC | 0 to +70°C | SMT | |
| ADS-946GM | -55 to +125°C | SMT | |
| ADS-946G/883 | -55 to +125°C | SMT | |

Receptacles for pc board mounting can be ordered through AMP, Inc., Part # 3-331272-8 (Component Lead Socket), 24 required. For MIL-STD-883 product specification, contact DATEL.