

256K x 16 (4-MBIT) DYNAMIC RAM WITH FAST PAGE MODE

JUNE 2007

FEATURES

- · Fast access and cycle time
- TTL compatible inputs and outputs
- Refresh Interval: 512 cycles/8 ms
- Refresh Mode: RAS-Only, CAS-before-RAS (CBR), and Hidden
- · JEDEC standard pinout
- Single power supply: 3.3V ± 10%
- Byte Write and Byte Read operation via two CAS
- · Lead-free available

DESCRIPTION

The *ISSI* IS41LV16257B is 262,144 x 16-bit high-performance CMOS Dynamic Random Access Memories. Fast Page Mode allows 512 random accesses within a single row with access cycle time as short as 12 ns per 16-bit word. The Byte Write control, of upper and lower byte, makes these devices ideal for use in 16- and 32-bit wide data bus systems.

These features make the IS41LV16257B ideally suited for high band-width graphics, digital signal processing, high-performance computing systems, and peripheral applications.

The IS41LV16257B is packaged in a 40-pin, 400-mil SOJ and TSOP (Type II).

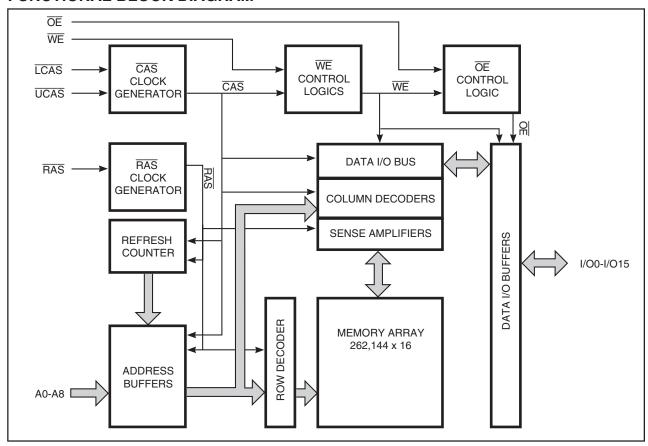
KEY TIMING PARAMETERS

Parameter	-35	-60	Unit	
Max. RAS Access Time (trac)	35	60	ns	
Max. CAS Access Time (tcac)	11	15	ns	
Max. Column Address Access Time (taa)	18	30	ns	
Min. Fast Page Mode Cycle Time (tpc)	14	25	ns	
Min. Read/Write Cycle Time (tnc)	60	110	ns	

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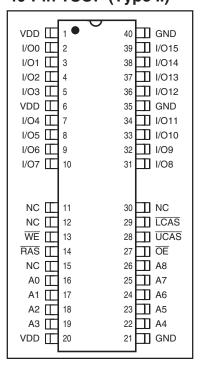


FUNCTIONAL BLOCK DIAGRAM

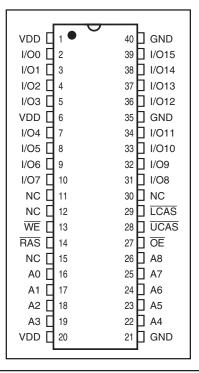


PIN CONFIGURATIONS

40-Pin TSOP (Type II)



40-Pin SOJ



PIN DESCRIPTIONS

A0-A8	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
WE	Write Enable
ŌĒ	Output Enable
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
V _{DD}	Power
GND	Ground
NC	No Connection



TRUTH TABLE

Function	RAS	LCAS	UCAS	WE	ŌĒ	Address tr/tc	I/O
Standby	Н	Н	Н	Χ	Χ	Χ	High-Z
Read: Word	L	L	L	Н	L	ROW/COL	Dout
Read: Lower Byte	L	L	Н	Н	L	ROW/COL	Lower Byte, Dout Upper Byte, High-Z
Read: Upper Byte	L	Н	L	Н	L	ROW/COL	Lower Byte, High-Z Upper Byte, Douт
Write: Word (Early Write)	L	L	L	L	Х	ROW/COL	Din
Write: Lower Byte (Early Write)) L	L	Н	L	Χ	ROW/COL	Lower Byte, DIN Upper Byte, High-Z
Write: Upper Byte (Early Write)) L	Н	L	L	Х	ROW/COL	Lower Byte, High-Z Upper Byte, DIN
Read-Write ^(1,2)	L	L	L	HØL	LØH	ROW/COL	Dout, Din
Hidden Refresh ²⁾	Read LØHØL	L	L	Н	L	ROW/COL	Douт
	Write LØHØL	L	L	L	Χ	ROW/COL	Douт
RAS-Only Refresh	L	Н	Н	Χ	Χ	ROW/NA	High-Z
CBR Refresh ⁽³⁾	HØL	L	L	Х	Х	Х	High-Z

- These WRITE cycles may also be BYTE WRITE cycles (either LCAS or UCAS active).
 These READ cycles may also be BYTE READ cycles (either LCAS or UCAS active).
 At least one of the two CAS signals must be active (LCAS or UCAS).



FUNCTIONAL DESCRIPTION

The IS41LV16257B is a CMOS DRAM optimized for high-speed bandwidth, low-power applications. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits. These are entered nine bits (A0-A8) at a time. The row address is latched by the Row Address Strobe (\overline{RAS}). The column address is latched by the Column Address Strobe (\overline{CAS}). \overline{RAS} is used to latch the first nine bits and \overline{CAS} is used to latch the latter nine bits.

The IS41LV16257B has two CAS controls, LCAS and UCAS. The LCAS and UCAS inputs internally generate a CAS signal functioning in an identical manner to the single CAS input on the other 256Kx16DRAMs. The key difference is that each CAS controls its corresponding I/O tristate logic (in conjunction with OE and WE and RAS). LCAS controls I/O0 - I/O7 and UCAS controls I/O8 - I/O15.

The IS41LV16257B CAS function is determined by the first CAS (LCAS or UCAS) transitioning LOW and the last transitioning back HIGH. The two CAS controls give the IS41LV16257B both BYTE READ and BYTE WRITE cycle capabilities.

Memory Cycle

A memory cycle is initiated by bringing \overline{RAS} LOW and it is terminated by returning both \overline{RAS} and \overline{CAS} HIGH. To ensure proper device operation and data integrity any memory cycle, once initiated, must not be ended or aborted before the minimum tras time has expired. A new cycle must not be initiated until the minimum precharge time trap, top has elapsed.

Read Cycle

A read cycle is initiated by the falling edge of \overline{CAS} or \overline{OE} , whichever occurs last, while holding \overline{WE} HIGH. The column address must be held for a minimum time specified by tar. Data Out becomes valid only when trac, tar, tare and toer are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters.

Write Cycle

A write cycle is initiated by the falling edge of $\overline{\text{CAS}}$ and $\overline{\text{WE}}$, whichever occurs last. The input data must be valid at or before the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$, whichever occurs last.

Refresh Cycle

To retain data, 512 refresh cycles are required in each 8 ms period. There are two ways to refresh the memory:

- By clocking each of the 512 row addresses (A0 through A8) with RAS at least once every 8 ms. Any read, write, read-modify-write or RAS-only cycle refreshes the addressed row.
- Using a CAS-before-RAS refresh cycle. CAS-before-RAS refresh is activated by the falling edge of RAS, while holding CAS LOW. In CAS-before-RAS refresh cycle, an internal 9-bit counter provides the row addresses and the external address inputs are ignored.

CAS-before-RAS is a refresh-only mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle.

Power-On

After application of the VDD supply, an initial pause of 200 µs is required followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS signal).

During power-on, it is recommended that \overline{RAS} track with V_{DD} or be held at a valid V_{IH} to avoid current surges.



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating	Unit
VT	Voltage on Any Pin Relative to GND	3.3V	-0.5 t0 +4.6	V
VDD	Supply Voltage	3.3V	-0.5 t0 +4.6	V
Іоит	Output Current		50	mA
Po	Power Dissipation		1	W
Та	Operation Temperature	Com.	0 to +70	°C
		Ind.	-40 to +85	
Tstg	Storage Temperature		-55 to +125	°C

Note:

RECOMMENDED OPERATING CONDITIONS (Voltages are referenced to GND)

Symbol	Parameter	Voltage	Min.	Тур.	Max.	Unit
VDD	Supply Voltage	3.3V	3.0	3.3	3.6	V
VIH	Input High Voltage	3.3V	2.0	_	V _{DD} + 0.3	V
VIL	Input Low Voltage	3.3	-0.3	_	8.0	V
TA	Ambient Temperature	Com.	0	_	70	°C
		Ind.	-40	_	85	

CAPACITANCE(1,2)

Symbol	Parameter	Max.	Unit
CIN1	Input Capacitance: A0-A8	5	pF
CIN2	Input Capacitance: RAS, UCAS, LCAS, WE, OE	7	pF
Сю	Data Input/Output Capacitance: I/O0-I/O15	7	pF

- 1. Tested initially and after any design or process changes that may affect these parameters.
- 2. Test conditions: $T_A = 25^{\circ}C$, f = 1 MHz, $V_{DD}=3.3V \pm 10\%$.

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



ELECTRICAL CHARACTERISTICS(1) (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition		Speed	Min.	Max.	Unit
lıL	Input Leakage Current	Any input $0V \le VIN \le VDD$ Other inputs not under test = $0V$			-10	10	μΑ
lio	Output Leakage Current	Output is disabled (Hi-Z) 0V ≤ Vouт ≤ VDD			-10	10	μΑ
Vон	Output High Voltage Level	lон = −2 mA			2.4	_	V
Vol	Output Low Voltage Level	IoL = +2 mA			_	0.4	V
Icc1	Stand-by Current: TTL	RAS, LCAS, UCAS ≥ VIH	Com.	3.3V	_	4	mA
lcc2	Stand-by Current: CMOS	$\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}} \ge V_{DD} - 0.2V$		3.3V	_	1	mA
Icc3	Operating Current: Random Read/Write ^(2,3,4) Average Power Supply Current	RAS, LCAS, UCAS, Address Cycling, tRC = tRC (min.)		-35 -60	_	230 170	mA
Icc4	Operating Current: Fast Page Mode ^(2,3,4) Average Power Supply Current	RAS = VIL, LCAS, UCAS, Cycling tpc = tpc (min.)		-35 -60	_	220 160	mA
lcc5	Refresh Current: RAS-Only ^(2,3) Average Power Supply Current	$\overline{\text{RAS}}$ Cycling, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}} \ge \text{V}_{\text{IH}}$ that $= \text{that}$ (min.)		-35 -60	_	230 170	mA
Icc6	Refresh Current: CBR ^(2,3,5) Average Power Supply Current	RAS, LCAS, UCAS Cycling trc = trc (min.)		-35 -60	_	230 170	mA

^{1.} An initial pause of 200 µs is required after power-up followed by eight \overline{RAS} refresh cycles (\overline{RAS} -Only or CBR) before proper device operation is assured. The eight \overline{RAS} cycles wake-up should be repeated any time the tree refresh requirement is exceeded.

^{2.} Dependent on cycle rates.

^{3.} Specified values are obtained with minimum cycle time and the output open.

^{4.} Column-address is changed once each fast page cycle.

^{5.} Enables on-chip refresh and address counters.



AC CHARACTERISTICS(1,2,3,4,5,6) (Recommended Operating Conditions unless otherwise noted.)

		-	35	_	60	
Symbol	Parameter		Max.		Max.	Units
trc	Random READ or WRITE Cycle Time	70	_	110	_	ns
trac	Access Time from RAS(6, 7)	_	35	_	60	ns
tcac	Access Time from CAS(6, 8, 15)	_	11	_	15	ns
taa	Access Time from Column-Address ⁽⁶⁾	_	18	_	30	ns
tras	RAS Pulse Width	35	10K	60	10K	ns
trp	RAS Precharge Time	25	_	40	_	ns
tcas	CAS Pulse Width(26)	6	10K	10	10K	ns
tcp	CAS Precharge Time ^(9, 25)	6	_	10	_	ns
tcsh	CAS Hold Time (21)	35	_	60	_	ns
trcd	RAS to CAS Delay Time(10, 20)	13	24	20	45	ns
tasr	Row-Address Setup Time	0	_	0	_	ns
trah	Row-Address Hold Time	6	_	10	_	ns
tasc	Column-Address Setup Time(20)	0	_	0	_	ns
tcah	Column-Address Hold Time(20)	6	_	10	_	ns
tar	Column-Address Hold Time (referenced to RAS)	30	_	45	_	ns
trad	RAS to Column-Address Delay Time(11)	12	20	15	30	ns
tral	Column-Address to RAS Lead Time	18	_	30	_	ns
trpc	RAS to CAS Precharge Time	0	_	0	_	ns
trsh	RAS Hold Time ⁽²⁷⁾	10	_	15	_	ns
tcLZ	CAS to Output in Low-Z(15, 29)	3	_	3	_	ns
tcrp	CAS to RAS Precharge Time(21)	5	_	5	_	ns
top	Output Disable Time(19, 28, 29)	3	15	3	15	ns
toe	Output Enable Time(15, 16)	_	11	_	15	ns
toehc	OE HIGH Hold Time from CAS HIGH	8	_	8	_	ns
toep	OE HIGH Pulse Width	8	_	8	_	ns
toes	OE LOW to CAS HIGH Setup Time	5	_	7	_	ns
trcs	Read Command Setup Time(17, 20)	0	_	0	_	ns
trrh	Read Command Hold Time (referenced to RAS) ⁽¹²⁾	0	_	0	_	ns
trch	Read Command Hold Time (referenced to CAS)(12, 17, 21)	0	_	0	_	ns
twch	Write Command Hold Time(17, 27)	5	_	10	_	ns
twcr	Write Command Hold Time (referenced to RAS)(17)	30	_	50	_	ns
twp	Write Command Pulse Width(17)	5	_	10	_	ns
twpz	WE Pulse Widths to Disable Outputs	10	_	10	_	ns
trwL	Write Command to RAS Lead Time(17)	10	_	15	_	ns
tcwL	Write Command to CAS Lead Time(17, 21)	8	_	15	_	ns
twcs	Write Command Setup Time(14, 17, 20)	0	_	0	_	ns
tohr	Data-in Hold Time (referenced to RAS)	30	_	46	_	ns

(Continued)



AC CHARACTERISTICS(1,2,3,4,5,6) (Recommended Operating Conditions unless otherwise noted.)

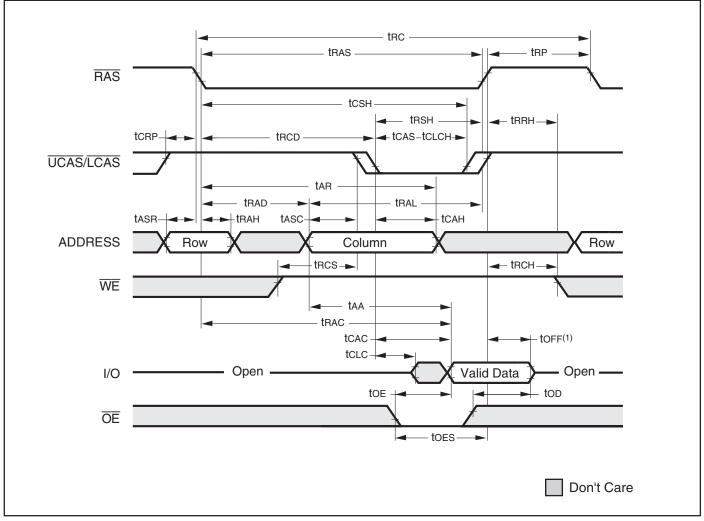
		-3	35	-6	0	
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
tach	Column-Address Setup Time to CAS Precharge during WRITE Cycle	15	_	15	_	ns
t OEH	OE Hold Time from WE during READ-MODIFY-WRITE cycle ⁽¹⁸⁾	8	_	15	_	ns
tos	Data-In Setup Time(15, 22)	0	_	0	_	ns
ton	Data-In Hold Time(15, 22)	6	_	10	_	ns
trwc	READ-MODIFY-WRITE Cycle Time	80	_	140	_	ns
trwd	RAS to WE Delay Time during READ-MODIFY-WRITE Cycle ⁽¹⁴⁾	46	_	80	_	ns
tcwp	CAS to WE Delay Time(14, 20)	25	_	36	_	ns
tawd	Column-Address to WE Delay Time(14)	30	_	49	_	ns
tpc	Fast Page Mode READ or WRITE Cycle Time(24)	14	_	25	_	ns
trasp	RAS Pulse Width	35	100K	60	100K	ns
t CPA	Access Time from CAS Precharge(15)	_	20	_	35	ns
tprwc	READ-WRITE Cycle Time(24)	45	_	60	_	ns
toff	Output Buffer Turn-Off Delay from CAS or RAS (13,15,19,29)	3	10	3	15	ns
twnz	Output Disable Delay from WE	3	10	3	15	ns
tclch	Last CAS going LOW to First CAS returning HIGH(23)	10	_	10	_	ns
tcsr	CAS Setup Time (CBR REFRESH)(30, 20)	8	_	10	_	ns
tchr	CAS Hold Time (CBR REFRESH)(30, 21)	8		10	_	ns
tord	OE Setup Time prior to RAS during HIDDEN REFRESH Cycle	0	_	0	_	ns
tref	Refresh Period (512 Cycles)	_	8	_	8	ms
tr	Transition Time (Rise or Fall)(2, 3)	2	50	2	50	ns



- 1. An initial pause of 200 µs is required after power-up followed by eight RAS refresh cycle (RAS-Only or CBR) before proper device operation is assured. The eight RAS cycles wake-up should be repeated any time the tREF refresh requirement is exceeded.
- Vi⊢ (MIN) and Vi⊢ (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between Vi⊢ and VIL (or between VIL and VIH) and assume to be 1 ns for all inputs.
- In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
- If $\overline{\text{CAS}}$ and $\overline{\text{RAS}} = V_{\text{IH}}$, data output is High-Z.
- 5. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
- 6. Measured with a load equivalent to one TTL gate and 50 pF.
- 7. Assumes that tRCD ≤ tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
- 8. Assumes that tRCD ≥ tRCD (MAX).
- 9. If CAS is LOW at the falling edge of RAS, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, CAS and RAS must be pulsed for tcp.
- 10. Operation with the trop (MAX) limit ensures that trac (MAX) can be met. trop (MAX) is specified as a reference point only; if trop is greater than the specified thoo (MAX) limit, access time is controlled exclusively by toac.
- 11. Operation within the trad (MAX) limit ensures that trad (MAX) can be met. trad (MAX) is specified as a reference point only; if trad is greater than the specified trad (MAX) limit, access time is controlled exclusively by taa.
- 12. Either trich or trich must be satisfied for a READ cycle.
- 13. toff (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to Voh or Vol.
- 14. twcs, trwb, tawb and tcwb are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If twcs ≥ twcs (MIN), the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If trwb ≥ trwb (MIN), tawb ≥ tawb (MIN) and tcwb ≥ tcwb (MIN), the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until \overline{CAS} and \overline{RAS} or \overline{OE} go back to ViH) is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW result in a LATE WRITE (OE-controlled) cycle.
- 15. Output parameter (I/O) is referenced to corresponding CAS input, I/O0-I/O7 by LCAS and I/O8-I/O15 by UCAS.
- 16. During a READ cycle, if OE is LOW then taken HIGH before CAS goes HIGH, I/O goes open. If OE is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
- 17. Write command is defined as \overline{WE} going low.
- 18. LATE WRITE and READ-MODIFY-WRITE cycles must have both top and toen met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if CAS remains LOW and OE is taken back to LOW after toeh is met.
- 19. The I/Os are in open during READ cycles once top or toff occur.
- 20. The first $\chi \overline{CAS}$ edge to transition LOW.
- 21. The last $\chi \overline{CAS}$ edge to transition HIGH.
- 22. These parameters are referenced to CAS leading edge in EARLY WRITE cycles and WE leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
- 23. Last falling $\chi \overline{\text{CAS}}$ edge to first rising $\chi \overline{\text{CAS}}$ edge.
- 24. Last rising $\chi \overline{\text{CAS}}$ edge to next cycle's last rising $\chi \overline{\text{CAS}}$ edge.
- 25. Last rising $\chi \overline{CAS}$ edge to first falling $\chi \overline{CAS}$ edge.
- 26. Each χCAS must meet minimum pulse width.
- 27. Last $\chi \overline{\text{CAS}}$ to go LOW.
- 28. I/Os controlled, regardless UCAS and LCAS.
- 29. The 3 ns minimum is a parameter guaranteed by design.
- 30. Enables on-chip refresh and address counters.



FAST-PAGE-MODE READ CYCLE

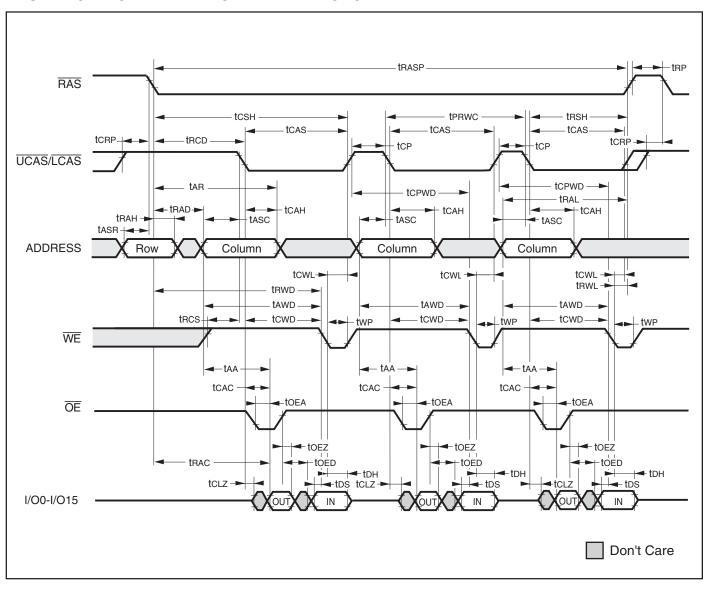


Note:

1. toff is referenced from rising edge of $\overline{\text{CAS}}$.

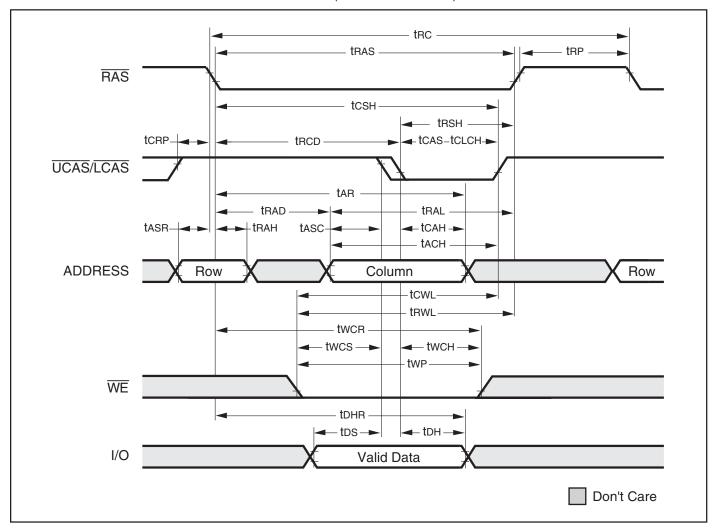


FAST PAGE MODE READ-MODIFY-WRITE CYCLE



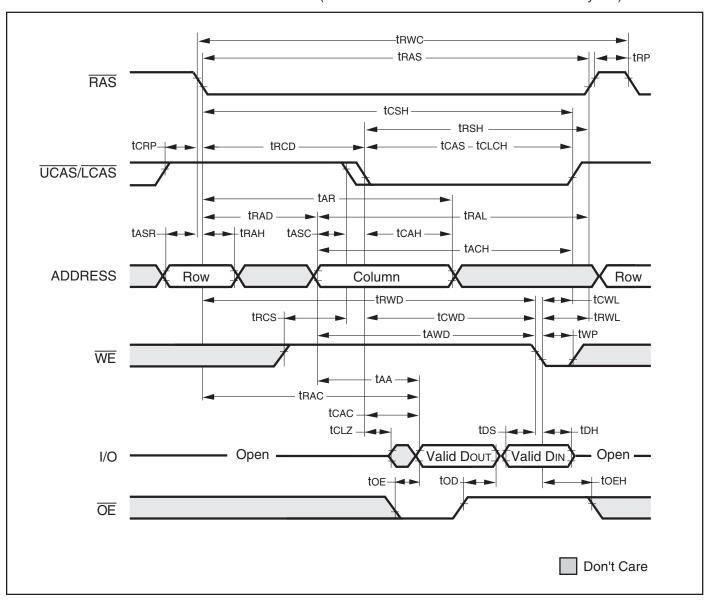


FAST-PAGE-MODE EARLY WRITE CYCLE (OE = DON'T CARE)



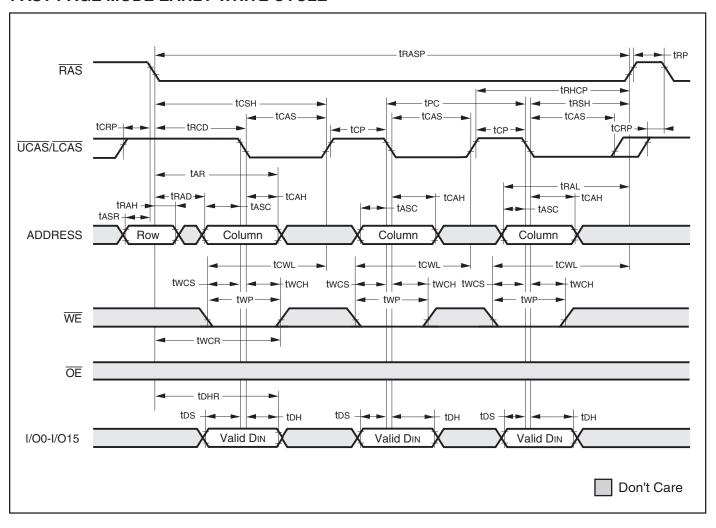


FAST-PAGE-MODE READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)





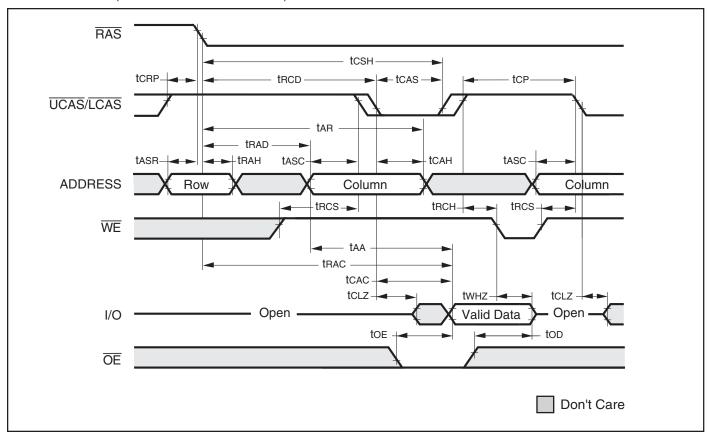
FAST PAGE MODE EARLY WRITE CYCLE



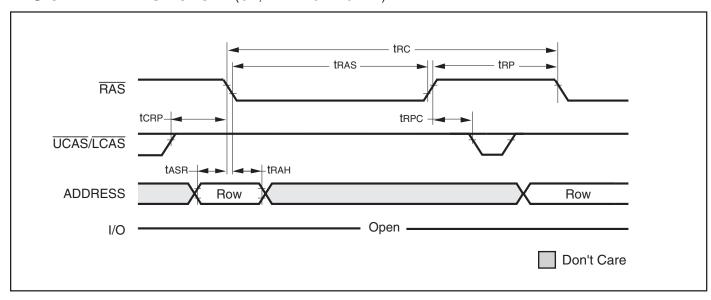


AC WAVEFORMS

READ CYCLE (With WE-Controlled Disable)

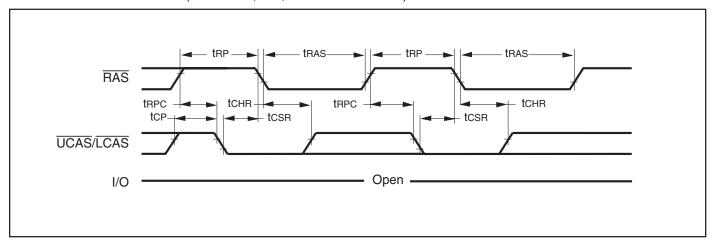


RAS-ONLY REFRESH CYCLE (OE, WE = DON'T CARE)

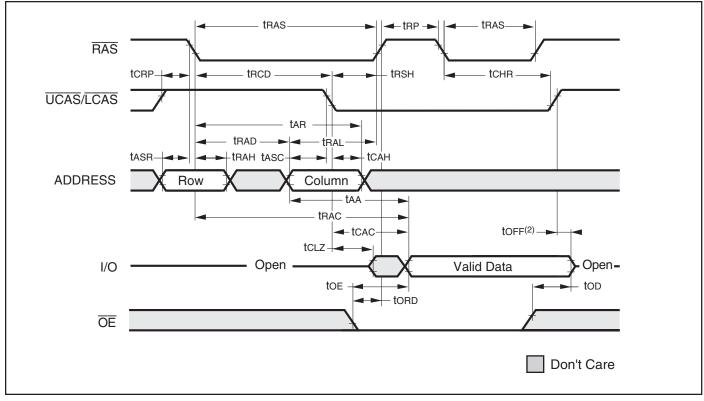




CBR REFRESH CYCLE (Addresses; WE, OE = DON'T CARE)



HIDDEN REFRESH CYCLE(1) (WE = HIGH; OE = LOW)



- A Hidden Refresh may also be performed after a Write Cycle. In this case, WE = LOW and OE = HIGH.
 toff is referenced from rising edge of RAS or CAS, whichever occurs last.



ORDERING INFORMATION:

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
35	IS41LV16257B-35K	400-mil SOJ
	IS41LV16257B-35KL	400-mil SOJ, Lead-free
	IS41LV16257B-35T	400-mil TSOP (Type II)
	IS41LV16257B-35TL	400-mil TSOP (Type II), Lead-free
60	IS41LV16257B-60K	400-mil SOJ
	IS41LV16257B-60KL	400-mil SOJ, Lead-free
	IS41LV16257B-60T	400-mil TSOP (Type II)
	IS41LV16257B-60TL	400-mil TSOP (Type II), Lead-free

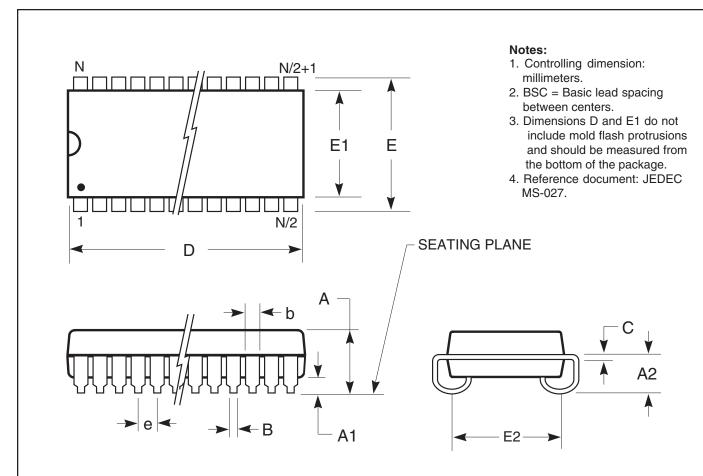
Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
35	IS41LV16257B-35KLI	400-mil SOJ, Lead-free

PACKAGING INFORMATION



400-mil Plastic SOJ Package Code: K



	Millim	eters	Inche	es	Millim	eters	Inche	es	Millin	neters	Inch	es
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads	(N)	28				3	2				36	
Α	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	_	0.025	_	0.64	_	0.025	_	0.64	_	0.025	_
A2	2.08	_	0.082	_	2.08	_	0.082	_	2.08	_	0.082	_
В	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
С	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	18.29	18.54	0.720	0.730	20.82	21.08	0.820	0.830	23.37	23.62	0.920	0.930
Е	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40	BSC	0.370) BSC	9.40	BSC	0.370) BSC	9.40	BSC	0.370	BSC
е	1.27	BSC	0.05	0 BSC	1.27 E	3SC	0.050) BSC	1.27	BSC	0.050) BSC

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PACKAGING INFORMATION



	Millimeters		Inches		Millim	Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
No. Leads	(N)	4	0			42	2				44		
Α	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	
A1	0.64	_	0.025	_	0.64	_	0.025	_	0.64	_	0.025	_	
A2	2.08	_	0.082	_	2.08	_	0.082	_	2.08	_	0.082	_	
В	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	
С	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	
D	25.91	26.16	1.020	1.030	27.18	27.43	1.070	1.080	28.45	28.70	1.120	1.130	
Е	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	
E2	9.40	BSC	0.370	BSC	9.40	BSC	0.370) BSC	9.40	BSC	0.370	BSC	
е	1.27	BSC	0.05	0 BSC	1.27 l	3SC	0.050) BSC	1.27	BSC	0.050) BSC	

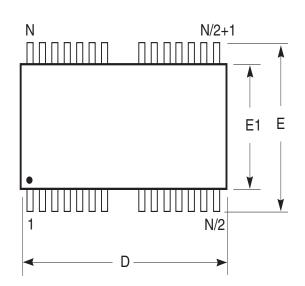
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PACKAGING INFORMATION

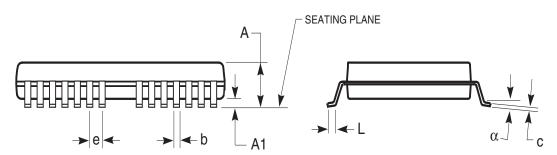


Plastic TSOP

Package Code: T (Type II)



- 1. Controlling dimension: millimeters, unless otherwise specified.
- BSC = Basic lead spacing between centers.
 Dimensions D1 and E do not include mold flash protrusions and should be measured from the bottom of the
- 4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II) (MS 25)							
	Millim	eters	Inch	nes			
Symbol	Min	Max Min		Max			
Ref. Std.							
N	24/26						
Α		1.20		0.0472			
A1	0.05	0.15	0.002	0.0059			
b	0.30	0.51	0.012	0.0201			
С	0.12	0.21	0.005	0.0083			
D	17.01	17.27	0.670	0.6899			
E ₁	7.49	7.75	0.295	0.3051			
е	1.27	BSC	0.05	0.050 BSC			
Е	9.02	9.42	0.462	0.4701			
L	0.40	0.60	0.016	0.0236			
α	0°	5°	0°	5°			

Plastic TSOP (T - Type II) (MS 24)							
	Millim	eters	Inch	es			
Symbol	Min	Max	Min	Max			
Ref. Std.							
N	40/44						
Α		1.20		0.0472			
A1	0.05	0.15	0.002	0.0059			
b	0.30	0.45	0.012	0.0157			
С	0.12	0.21	0.005	0.0083			
D	18.31	18.51	0.721	0.7287			
E ₁	10.06	10.26	0.396	0.4040			
е	0.80	BSC	0.03	I BSC			
Е	11.56	11.96	0.455	0.4709			
L	0.40	0.60	0.016	0.0236			
α	0°	8°	0°	8°			

Plastic TSOP (T - Type II) (MS 24)							
	Millim	eters	Inc	Inches			
Symbol	Min	Max	Min	Max			
Ref. Std.							
N		4	4/50				
Α		1.20		0.0472			
A1	0.05	0.15	0.002	0.0059			
b	0.30	0.45	0.012	0.0157			
С	0.12	0.21	0.005	0.0083			
D	20.85	21.05	0.821	0.8287			
E ₁	10.06	10.26	0.396	0.4040			
е	0.80	BSC	0.03	0.031 BSC			
Е	11.56	11.96	0.455	0.4709			
L	0.40	0.60	0.016	0.0236			
α	0°	8°	0°	8°			