

NB7L11M

2.5V/3.3V Differential 1:2 Clock/Data Fanout Buffer/ Translator with CML Outputs and Internal Termination

Description

The NB7L11M is a differential 1-to-2 clock/data distribution chip with internal source termination and CML output structure, optimized for low skew and minimal jitter. The device is functionally equivalent to the EP11, LVEP11, or SG11 devices. Device produces two identical output copies of clock or data operating up to 8 GHz or 12 Gb/s, respectively. As such, NB7L11M is ideal for SONET, GigE, Fiber Channel, Backplane and other clock/data distribution applications.

Inputs incorporate internal 50 Ω termination resistors and accept LVPECL, CML, LVCMOS, LVTTTL, or LVDS (See Table 6). Differential 16 mA CML output provides matching internal 50 Ω terminations, and 400 mV output swings when externally terminated, 50 Ω to V_{CC} (See Figure 14).

The device is offered in a low profile 3x3 mm 16-pin QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

Features

- Maximum Input Clock Frequency up to 8 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- < 0.5 ps of RMS Clock Jitter
- < 10 ps of Data Dependent Jitter
- 30 ps Typical Rise and Fall Times
- 110 ps Typical Propagation Delay
- 3 ps Typical Within Device Skew
- Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- CML Output Level (400 mV Peak-to-Peak Output) Differential Output Only
- 50 Ω Internal Input and Output Termination Resistors
- Functionally Compatible with Existing 2.5 V/3.3 V LVEL, LVEP, EP and SG Devices
- Pb-Free Packages are Available*

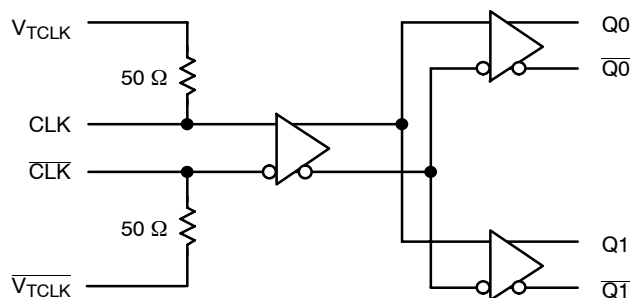


Figure 1. Logic Diagram



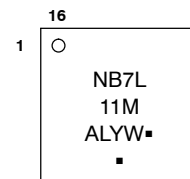
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM*



QFN-16
MN SUFFIX
CASE 485G



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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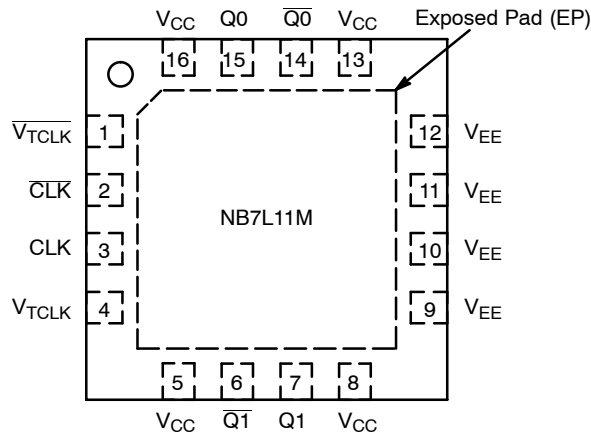


Figure 2. QFN-16 Pinout (Top View)

Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|------------|-----------------------|-----------------------------------|---|
| 1 | $\overline{V_{TCLK}}$ | - | Internal 50 Ω Termination Pin for \overline{CLK} |
| 2 | \overline{CLK} | LVPECL, CML, LVCMOS, LVTTTL, LVDS | Inverted Differential Clock/Data Input. (Note 1) |
| 3 | CLK | LVPECL, CML, LVCMOS, LVTTTL, LVDS | Noninverted Differential Clock/Data Input. (Note 1) |
| 4 | V_{TCLK} | - | Internal 50 Ω Termination Pin for CLK |
| 5,8,13,16 | V_{CC} | - | Positive Supply Voltage. All V_{CC} pins must be externally connected to a Power Supply to guarantee proper operation. |
| 6 | $\overline{Q1}$ | CML Output | Inverted \overline{CLK} output 1 with internal 50 Ω source termination resistor. (Note 2) |
| 7 | Q1 | CML Output | Noninverted CLK output 1 with internal 50 Ω source termination resistor. (Note 2) |
| 9,10,11,12 | V_{EE} | - | Negative Supply Voltage. All V_{EE} pins must be externally connected to a Power Supply to guarantee proper operation. |
| 14 | $\overline{Q0}$ | CML Output | Inverted \overline{CLK} output 0 with internal 50 Ω source termination resistor. (Note 2) |
| 15 | Q0 | CML Output | Noninverted CLK output 0 with internal 50 Ω source termination resistor. (Note 2) |
| - | EP | - | Exposed Pad. The thermally exposed pad on package bottom (see case drawing) must be attached to a heatsinking conduit. It is recommended to connect the EP to the lower potential (V_{EE}). |

1. In the differential configuration when the input termination pins (V_{TCLK} , $\overline{V_{TCLK}}$) are connected to a common termination voltage or left open, and if no signal is applied on CLK and \overline{CLK} then the device will be susceptible to self-oscillation.
2. CML outputs require 50 Ω receiver termination resistor to V_{CC} for proper operation.

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Table 2. ATTRIBUTES

| Characteristics | | Value | |
|--|---|-------------------------------|-------------|
| ESD Protection | Human Body Model Machine Model Charged Device Model | > 1500 V > 50 V > 500 V | |
| Moisture Sensitivity (Note 3) | | Pb Pkg | Pb-Free Pkg |
| | QFN-16 | Level 1 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| Transistor Count | | 285 | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

3. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------|---|---|-------------------------------|----------------------------|--|
| V_{CC} | Positive Power Supply | $V_{EE} = 0\text{ V}$ | | 3.6 | V |
| V_I | Input Voltage | $V_{EE} = 0\text{ V}$ | $V_{EE} \leq V_I \leq V_{CC}$ | 3.6 | V |
| V_{INPP} | Differential Input Voltage [CLK - $\overline{\text{CLK}}$] | $V_{CC} - V_{EE} \geq 2.8\text{ V}$ $V_{CC} - V_{EE} < 2.8\text{ V}$ | | 2.8 $ V_{CC} - V_{EE} $ | V |
| I_{IN} | Input Current Through R_T (50 Ω Resistor) | Static Surge | | 45 80 | mA mA |
| I_{out} | Output Current | Continuous Surge | | 25 50 | mA mA |
| T_A | Operating Temperature Range | QFN-16 | | -40 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}\text{C}$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) (Note 4) | 0 lfpm 500 lfpm | QFN-16 QFN-16 | 42 36 | $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | 2S2P (Note 4) | QFN-16 | 3 to 4 | $^{\circ}\text{C}/\text{W}$ |
| T_{sol} | Wave Solder Pb Pb-Free | | | 265 265 | $^{\circ}\text{C}$ |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

4. JEDEC standard multilayer board - 2S2P (2 signal, 2 power).

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Table 4. DC CHARACTERISTICS, CLOCK Inputs, CML Outputs ($V_{CC} = 2.375\text{ V to }3.465\text{ V}$, $V_{EE} = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$)
(Note 5)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|----------|---|----------------|----------------|----------------|------|
| I_{CC} | Power Supply Current (Input and Outputs open) | | 85 | 105 | mA |
| V_{OH} | Output HIGH Voltage (Note 6) | $V_{CC} - 60$ | $V_{CC} - 20$ | V_{CC} | mV |
| V_{OL} | Output LOW Voltage (Note 6) | $V_{CC} - 530$ | $V_{CC} - 420$ | $V_{CC} - 360$ | mV |

Differential Input Driven Single-Ended (see Figures 10 & 12) (Note 8)

| | | | | | |
|----------|--|---------------|--|---------------|----|
| V_{th} | Input Threshold Reference Voltage Range (Note 7) | 1125 | | $V_{CC} - 75$ | mV |
| V_{IH} | Single-ended Input HIGH Voltage (Note 8) | $V_{th} + 75$ | | V_{CC} | mV |
| V_{IL} | Single-ended Input LOW Voltage (Note 8) | V_{EE} | | $V_{th} - 75$ | mV |

Differential Inputs Driven Differentially (see Figures 11 & 13) (Note 8)

| | | | | | |
|------------------|--|----------|------|---------------|---------------------------------|
| V_{IHCLK} | Differential Input HIGH Voltage | 1200 | | V_{CC} | mV |
| V_{ILCLK} | Differential Input LOW Voltage | V_{EE} | | $V_{CC} - 75$ | mV |
| V_{CMR} | Input Common Mode Range (Differential Configuration) | 1163 | | $V_{CC} - 38$ | mV |
| V_{ID} | Differential Input Voltage ($V_{IHCLK} - V_{ILCLK}$) | 75 | | 2500 | mV |
| I_{IH} | Input HIGH Current CLK / \overline{CLK} ($V_{TCLK}/\sqrt{V_{TCLK}}$ Open) | 0 | 25 | 100 | μA |
| I_{IL} | Input LOW Current CLK / \overline{CLK} ($V_{TCLK}/\sqrt{V_{TCLK}}$ Open) | -10 | 0 | 10 | μA |
| R_{TIN} | Internal Input Termination Resistor | 45 | 50 | 55 | Ω |
| R_{TOUT} | Internal Output Termination Resistor | 45 | 50 | 55 | Ω |
| $R_{Temp\ Coef}$ | Internal I/O Termination Resistor Temperature Coefficient | | 6.38 | | $\text{m}\Omega/^\circ\text{C}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC} .
6. CML outputs require $50\ \Omega$ receiver termination resistors to V_{CC} for proper operation.
7. V_{th} is applied to the complementary input when operating in single-ended mode.
8. V_{CMR} min varies 1:1 with V_{EE} , V_{CMR} max varies 1:1 with V_{CC} .

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Table 5. AC CHARACTERISTICS ($V_{CC} = 2.375\text{ V to }3.465\text{ V}$, $V_{EE} = 0\text{ V}$; Note 9)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------|---|------------|---------------------------------|--------------------------------|------------|---------------------------------|--------------------------------|------------|---------------------------------|--------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OUTPP} | Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \leq 6\text{ GHz}$ (See Figure 3) $f_{in} \leq 8\text{ GHz}$ | 280 140 | 400 300 | | 280 140 | 400 300 | | 280 140 | 400 300 | | mV |
| f_{data} | Maximum Operating Data Rate | 10 | 12 | | 10 | 12 | | 10 | 12 | | Gb/s |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential | 70 | 110 | 150 | 70 | 110 | 150 | 70 | 110 | 150 | ps |
| t_{SKEW} | Duty Cycle Skew (Note 10) Within-Device Skew Device-to-Device Skew (Note 11) | | 2.0 3.0 20 | 5.0 15 50 | | 2.0 3.0 20 | 5.0 15 50 | | 2.0 3.0 20 | 5.0 15 50 | ps |
| t_{JITTER} | RMS Random Clock Jitter (Note 12) $f_{in} = 6\text{ GHz}$ $f_{in} = 8\text{ GHz}$ Peak/Peak Data Dependent Jitter $f_{in} = 2.488\text{ Gb/s}$ (Note 13) $f_{data} = 5\text{ Gb/s}$ $f_{data} = 10\text{ Gb/s}$ | | 0.2 0.2 2.0 3.0 5.0 | 0.5 0.5 5.0 8.0 10 | | 0.2 0.2 2.0 3.0 5.0 | 0.5 0.5 5.0 8.0 10 | | 0.2 0.2 2.0 3.0 5.0 | 0.5 0.5 5.0 8.0 10 | ps |
| V_{INPP} | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 14) | 75 | 400 | 2500 | 75 | 400 | 2500 | 75 | 400 | 2500 | mV |
| t_r t_f | Output Rise/Fall Times @ 1 GHz Q, \bar{Q} (20% – 80%) | | 30 | 60 | | 30 | 60 | | 30 | 60 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Measured by forcing V_{INPP} (TYP) from a 50% duty cycle clock source. All loading with an external $R_L = 50\ \Omega$ to V_{CC} . Input edge rates 40 ps (20% – 80%).
10. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw-} and T_{pw+} @1 GHz.
11. Device to device skew is measured between outputs under identical transition @ 1 GHz.
12. Additive RMS jitter with 50% duty cycle clock signal at 8 GHz & 10 GHz.
13. Additive peak-to-peak data dependent jitter with input NRZ data at PRBS $2^{23}-1$.
14. V_{INPP} (MAX) cannot exceed $V_{CC} - V_{EE}$. Input voltage swing is a single-ended measurement operating in differential mode.

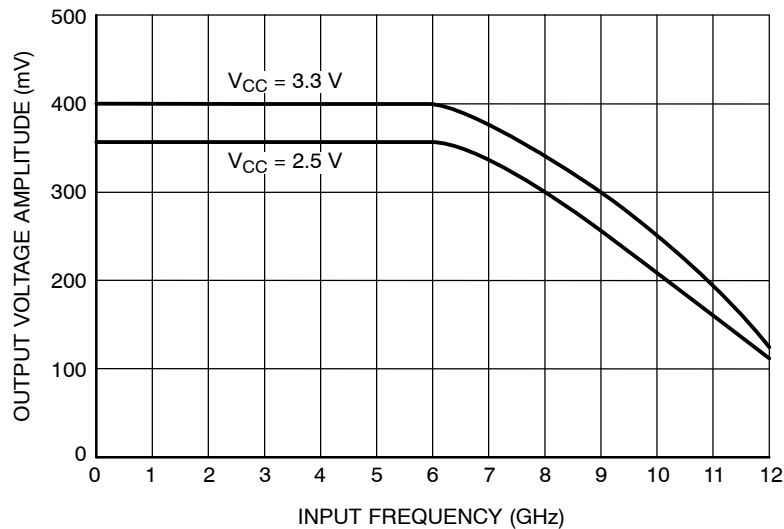


Figure 3. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{in}) at Ambient Temperature (Typical) ($V_{INPP} = 400\text{ mV}$)

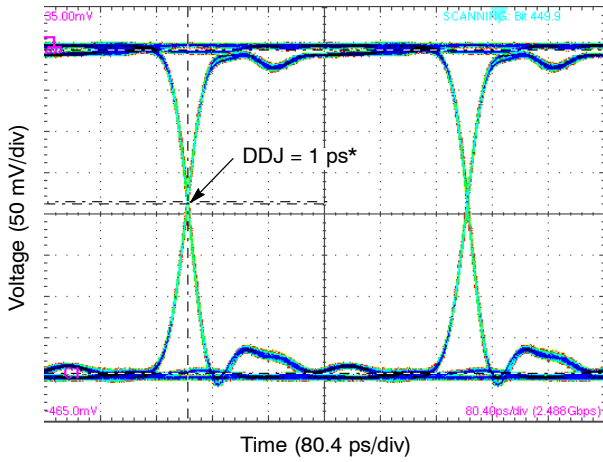


Figure 4. Typical Output Waveform at 2.488 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 75$ mV)

*Input signal DDJ = 6.4 ps

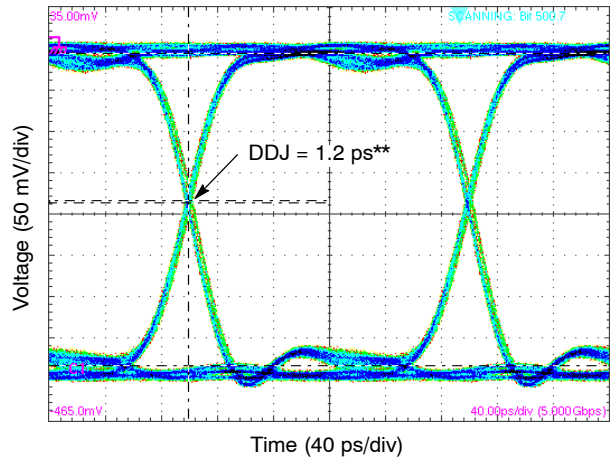


Figure 5. Typical Output Waveform at 5 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 75$ mV)

**Input signal DDJ = 7.2 ps

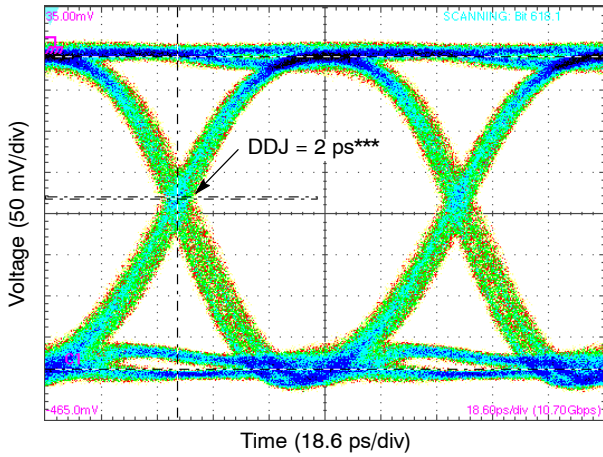


Figure 6. Typical Output Waveform at 10.7 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 75$ mV)

***Input signal DDJ = 11 ps

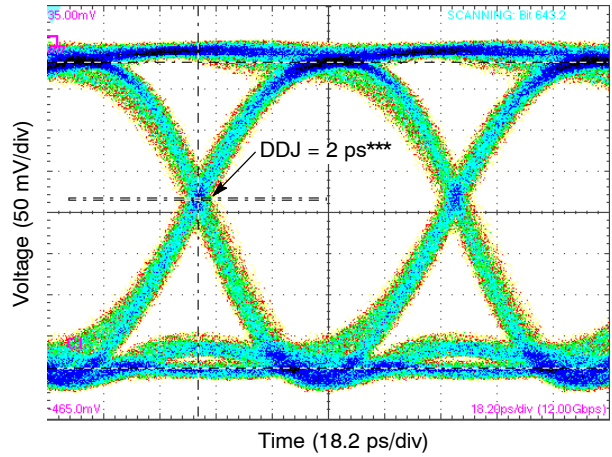


Figure 7. Typical Output Waveform at 12 Gb/s with PRBS $2^{23}-1$ ($V_{inpp} = 75$ mV)

***Input signal DDJ = 13 ps

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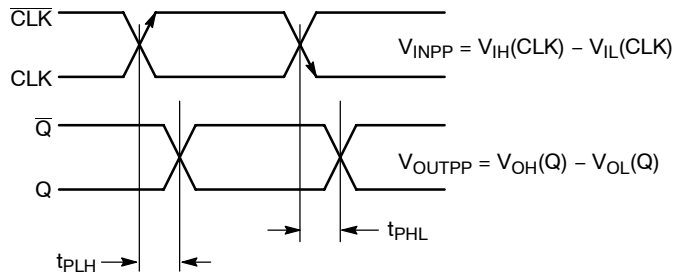


Figure 8. AC Reference Measurement

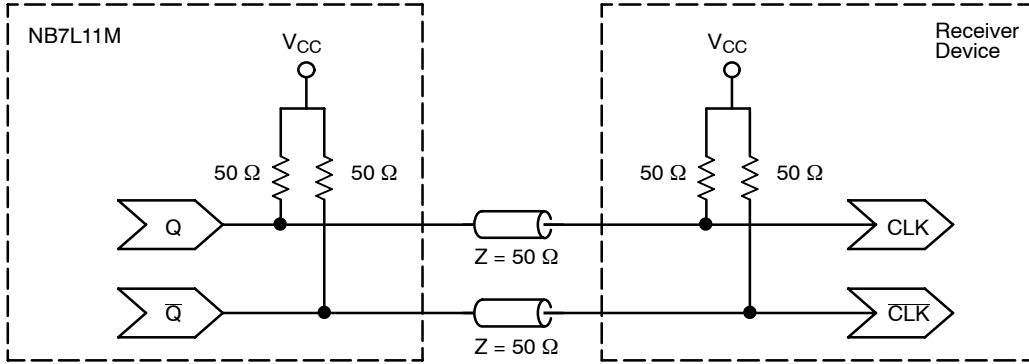


Figure 9. Typical Termination for Output Driver Using External Termination Resistor (Refer to Application Notes AND8020/D and AND8173/D)

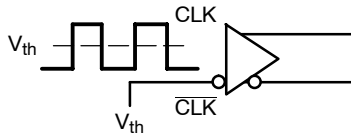


Figure 10. Differential Input Driven Single-Ended

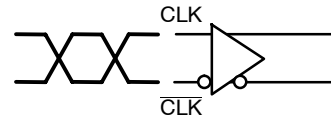


Figure 11. Differential Inputs Driven Differentially

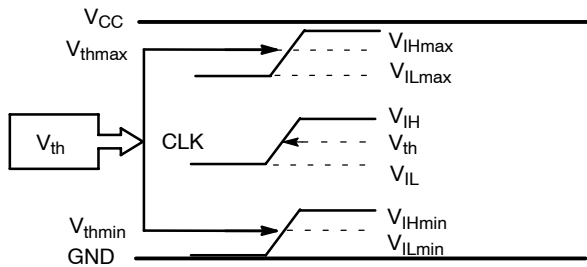


Figure 12. V_{th} Diagram

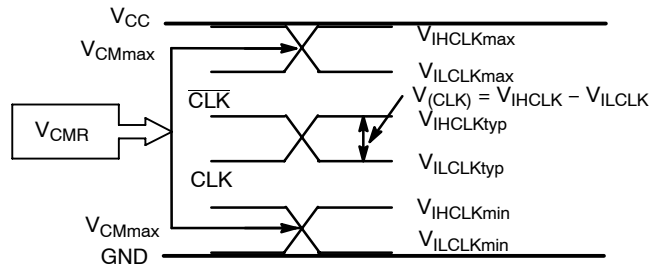


Figure 13. V_{CMR} Diagram

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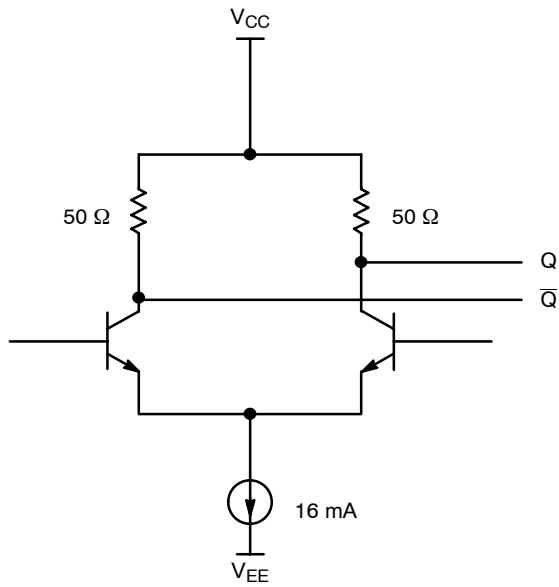


Figure 14. CML Output Structure

Table 6. INTERFACING OPTIONS

| INTERFACING OPTIONS | CONNECTIONS |
|---------------------|---|
| CML | Connect V_{TCLK} , $\overline{V_{TCLK}}$ to V_{CC} |
| LVDS | Connect V_{TCLK} , $\overline{V_{TCLK}}$ together CLK input |
| AC-COUPLED | Bias V_{TCLK} , $\overline{V_{TCLK}}$ Inputs within (V_{CMR}) Common Mode Range |
| RSECL, LVPECL | Standard ECL Termination Techniques. See AND8020/D. |
| LVTTTL, LVCMOS | An external voltage should be applied to the unused complementary differential input. Nominal voltage is 1.5 V for LVTTTL and $V_{CC}/2$ for LVCMOS inputs. |

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Application Information

All NB7L11M inputs can accept PECL, CML, LVTTTL, LVCMOS and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are

minimum input swing of 75 mV and the maximum input swing of 2500 mV. Within these conditions, the input voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a 50 Ω environment ($Z = 50 \Omega$).

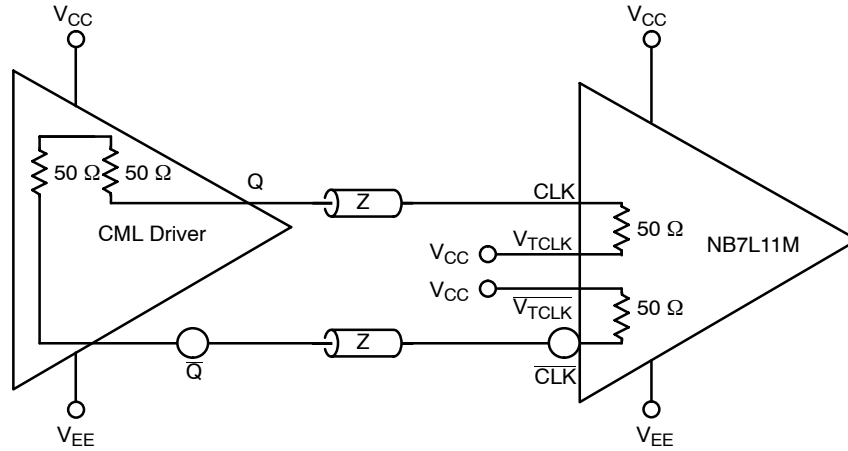


Figure 15. CML to CML Interface

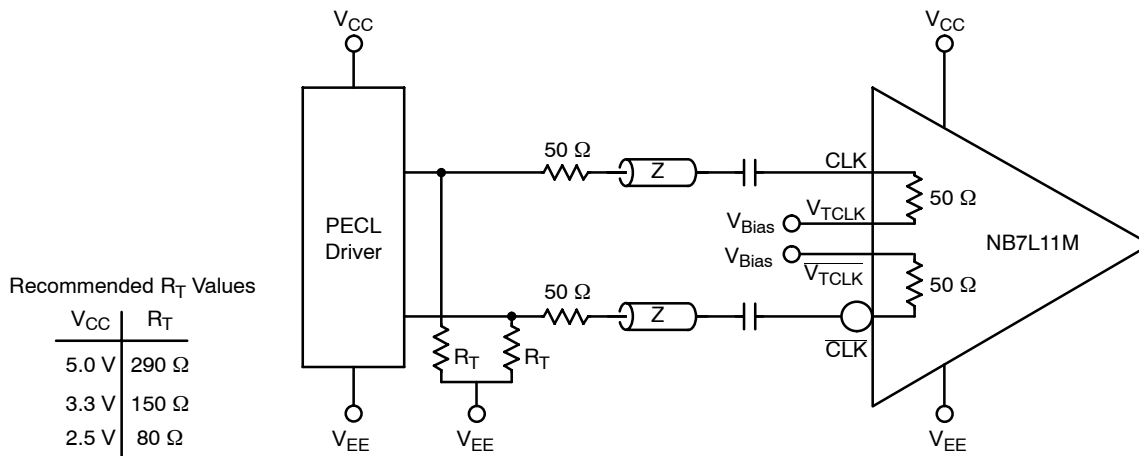


Figure 16. PECL to CML Receiver Interface

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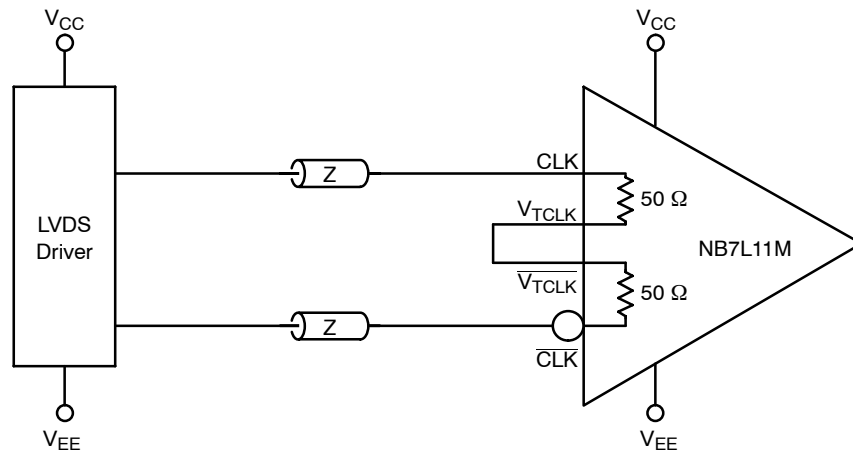


Figure 17. LVDS to CML Receiver Interface

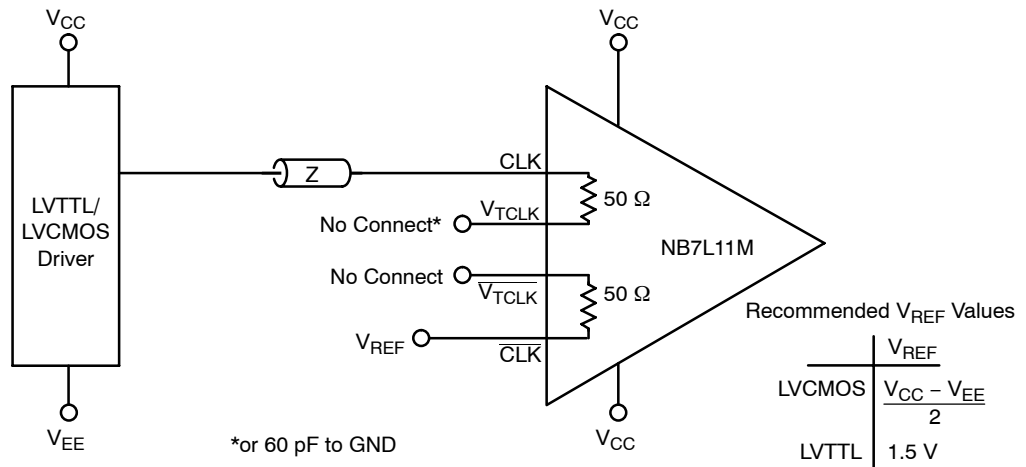


Figure 18. LVCMOS/LVTTL to CML Receiver Interface

ORDERING INFORMATION

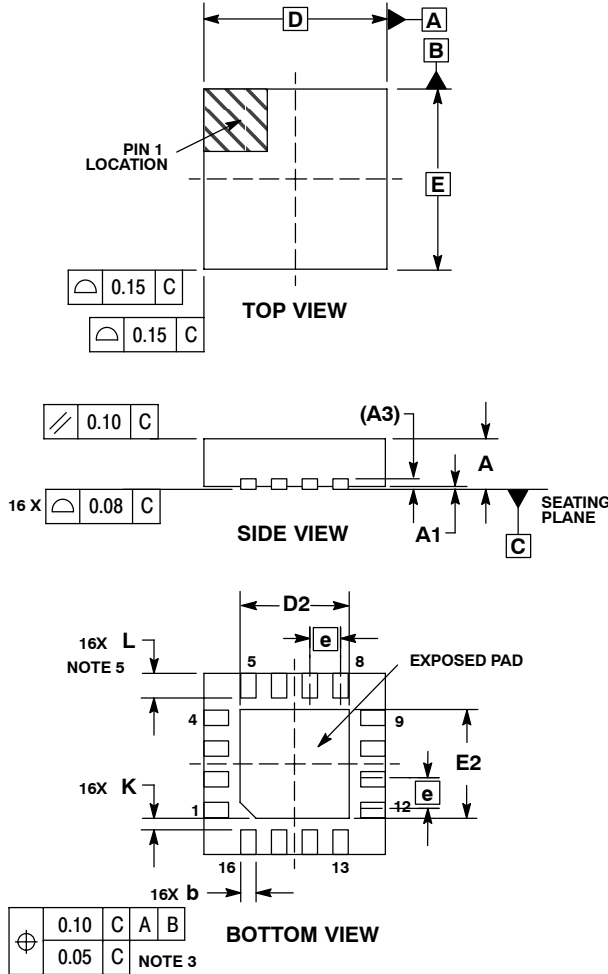
| Device | Package | Shipping† |
|--------------|---------------------|------------------|
| NB7L11MMN | QFN-16 | 123 Units/Rail |
| NB7L11MMNG | QFN-16 (Pb-Free) | 123 Units/Rail |
| NB7L11MMNR2 | QFN-16 | 3000 Tape & Reel |
| NB7L11MMNR2G | QFN-16 (Pb-Free) | 3000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB7L11M

PACKAGE DIMENSIONS

16 PIN QFN
MN SUFFIX
CASE 485G-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 3.00 | BSC |
| D2 | 1.65 | 1.85 |
| E | 3.00 | BSC |
| E2 | 1.65 | 1.85 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |

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