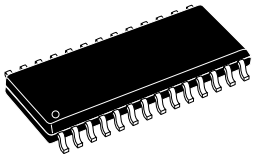
TDA7348

Digitally controlled audio processor

Features

- Input multiplexer
  - Three stereo and one mono inputs
  - Selectable input gain for optimal adaptation to different sources
- Volume control in 0.3db steps including gain up to 20dB
- Zero crossing mute and direct mute
- Pause detector with programmable threshold
- Soft mute controlled by software or hardware PIN
- Bass and treble control
- Four speaker attenuators
  - Four independent speakers control in 1.25dB steps for balance and fader facilities
  - Independent mute function
- All functions programmable via serial I^2C bus



SO-28

Description

The TDA7348 is an upgrade of the TDA7318 audioprocessor.

Thanks to the used BIPOLAR/CMOS technology, very low distortion, low noise and DC-stepping are obtained. Due to a highly linear signal processing, using CMOS-switching techniques instead of standard bipolar multipliers, very low distortion and very low noise are obtained Several new features like softmute, zero-crossing mute and pause detector are implemented.

The Soft Mute function can be activated in two ways, either via the serial bus (bit D0, Mute Byte), or directly on pin 22 through an I/O line of the microcontroller

Very low DC stepping is obtained by use of a BICMOS technology.

Order codes

Part number	Package	Packing
TDA7348D	SO-28	Tube
TDA7348D013TR	SO-28	Tape and reel
E-TDA7348D (1)	SO-28	Tube
E-TDA7348D013TR (1)	SO-28	Tape and reel

1. This device is Pb-free Ecopack , see *Chapter 5* Package information.

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1 Block diagram and PIN connections

Figure 1. Block diagram

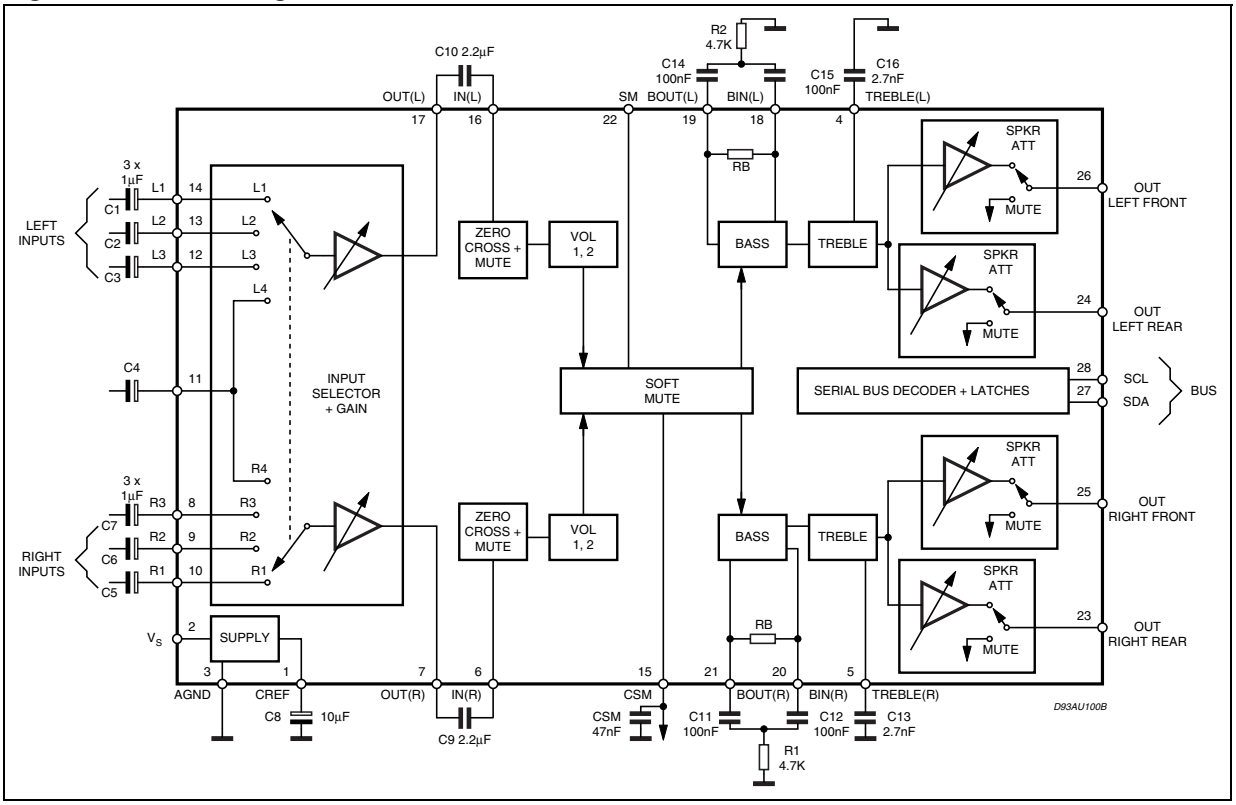
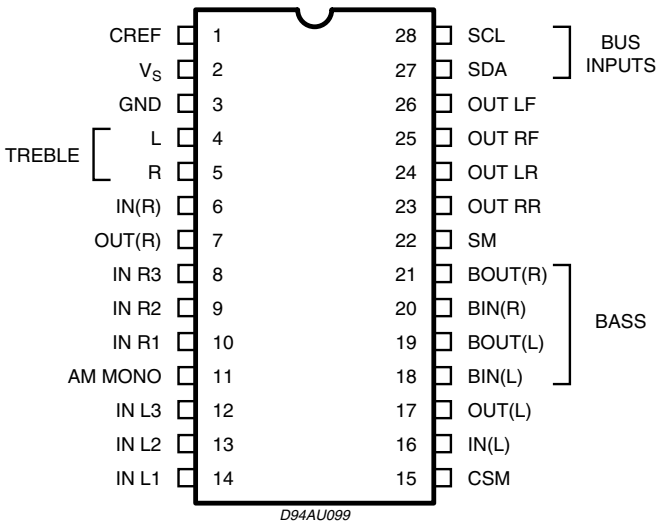


Figure 2. PIN connections



2 Electrical characteristics

Table 1. Electrical characteristics

V_S = 9V; R_L = 10KΩ; Rg = 50Ω; T_{amb} = 25°C; all controls flat (G = 0.3dB step 0dB); f = 1KHz. Refer to the test circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Input selector						
R_I	Input resistance		70	100	130	KΩ
V_{CL}	Clipping level	d ≤ 0.3%	2.1	2.6		V_{RMS}
S_I	Input separation		80	100		dB
R_L	Output load resistance		2			KΩ
$G_{I\ MIN}$	Minimum input gain		-0.75	0	0.75	dB
$G_{I\ MAX}$	Maximum input gain		10.25	11.25	12.25	dB
G_{step}	Step resolution		2.75	3.75	4.75	dB
e_N	Input noise	20Hz to 20 KHz unweighted		2.3		μV
V_{DC}	DC steps	Adiacent gain steps		1.5	10	mV
		G_{IMIN} to G_{IMAX}		3		mV
Volume control (1 + 2)						
R_I	Input resistance		35	50		KΩ
G_{MAX}	Maximum gain		18.75	20	21.25	dB
A_{MAX}	Maximum attenuation			78.45		dB
A_{STEPC}	Step resolution coarse attenuation		0.5	1.25	2.0	dB
A_{STEPF}	Step resolution fine attenuation		0.11	0.31	0.51	dB
E_A	Attenuation set error	G = 20 to -20dB	-1.25	0	1.25	dB
		G = -20 to -58dB	-3		2	dB
E_t	Tracking error				2	dB
V_{DC}	DC steps	Adiacent attenuation steps	-3	0	3	mV
		From 0dB to A_{MAX}		0.5	5	mV
Zero crossing mute						
V_{TH}	Zero crossing threshold	WIN = 11		20		mV
		WIN = 10		40		mV
		WIN = 01		80		mV
		WIN = 00		160		mV
A_{MUTE}	Mute attenuation		80	100		dB
V_{DC}	DC step	0dB to Mute		0	3	mV

Table 1. Electrical characteristics (continued)
V_S = 9V; R_L = 10KΩ; Rg = 50Ω; T_{amb} = 25°C; all controls flat (G = 0.3dB step 0dB); f = 1KHz. Refer to the test circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Soft mute						
A_{MUTE}	Mute attenuation		45	60		dB
T_{DON}	ON delay time	C_{CSM} = 22nF; 0 to -20dB; I = I_{MAX}	0.7	1	1.7	ms
		C_{CSM} = 22nF; 0 to -20dB; I = I_{MIN}	20	35	55	ms
T_{DOFF}	OFF delay time	V_{CSM} = 0V; I = I_{MAX}	25	50	75	µA
		V_{CSM} = 0V; I = I_{MIN}		1		µA
V_{THSM}	Soft mute threshold		1.5	2.5	3.5	V
R_{INT}	Pull-up resistor (pin 22)		35	50	65	KΩ
V_{SMH}	(pin 22) level high	Soft Mute active	3.5			V
V_{SML}	(pin 22) level low				1	V
Bass control						
B_{BOOST}	Max bass boost		15	18	20	dB
B_{CUT}	Max bass cut		-8.5	-10	-11.5	dB
A_{step}	Step resolution		1	2	3	dB
R_g	Internal feedback resistance		45	65	85	KΩ
Treble control						
C_{RANGE}	Control range		±13	±14	±15	dB
A_{step}	Step resolution		1	2	3	dB
Speaker attenuators						
C_{RANGE}	Control range		35	37.5	40	dB
A_{step}	Step resolution		0.5	1.25	2.0	dB
A_{MUTE}	Output mute attenuation	Data word = XXX11111	80	100		dB
E_A	Attenuation set error				1.25	dB
V_{DC}	DC steps	Adjacent attenuation steps		0	3	mV
Audio output						
V_{clip}	Clipping level	d = 0.3%	2.1	2.6		Vrms
R_L	Output load resistance		2			KΩ
R_O	Output impedance			30	100	W
V_{DC}	DC voltage level		3.5	3.8	4.1	V
General						
V_{CC}	Supply voltage		6	9	10.2	V

Table 1. Electrical characteristics (continued)
V_S = 9V; R_L = 10KΩ; Rg = 50Ω; T_{amb} = 25°C; all controls flat (G = 0.3dB step 0dB); f = 1KHz. Refer to the test circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC}	Supply current		5	10	15	mA
PSRR	Power supply rejection ratio	f = 1KHz	60	80		dB
		B = 20 to 20kHz "A" weighted		65		dB
eNO	Output noise	Output Muted (B = 20 to 20kHz flat)		2.5		µV
		All Gains 0dB (B = 20 to 20kHz flat)		5	15	µV
E_t	Total tracking error	A_V= 0 to -20dB		0	1	dB
		A_V= -20 to -60dB		0	2	dB
S/N	Signal to noise ratio	All Gains = 0dB; V_O= 1Vrms		106		dB
S_C	Channel separation		80	100		dB
d	Distortion	V_{in} = 1V		0.01	0.08	%
Bus inputs						
V_{IL}	Input low voltage				1	V
V_{IN}	Input high voltage		3			V
I_{IN}	Input current	V_{IN} = 0.4V	-5		5	µA
V_O	Output voltage SDA acknowledge	I_O = 1.6mA		0.4	0.8	V

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	10.5	V
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Table 3. Thermal data

Symbol	Parameter	SO28	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction pins	65	°C/W

Table 4. Quick reference data

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vs	Supply voltage	6	9	10.2	V
VCL	Max. input signal handling	2.1	2.6		Vrms
THD	Total harmonic distortion V = 1Vrms f = 1KHz		0.01	0.08	%
S/N	Signal to noise ratio		106		dB

Table 4. Quick reference data (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
S_C	Channel separation f = 1KHz		100		dB
	Volume control	-78.45		20	dB
	Treble control 2dB step	-14		+14	dB
	Bass control 2dB step	-10		+18	dB
	Fader and balance control 1.25dB step	-38.75		0	dB
	Input gain 3.75dB step	0		11.25	dB
	Mute attenuation		100		dB

3 I²C BUS interface

Data transmission from microprocessor to the TDA7348 and vice-versa takes place through the 2 wires of the I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to the positive supply voltage must be externally connected).

3.1 Data validity

As shown in *Figure 3.*, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

3.2 Start and stop conditions

As shown in *Figure 4.* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

A STOP conditions must be sent before each START condition.

3.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

3.4 Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 5.*). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

3.5 Transmission without acknowledgement

The microprocessor can use a simpler transmission, if it avoids detection of the acknowledgement from the audio processor. It simply waits one clock pulse without checking the slave acknowledgment, and sends the new data.

This approach of course is less protected from errors, increases the possibility of interference, and decreases the immunity to noise.

Figure 3. Data validity on the I²C BUS

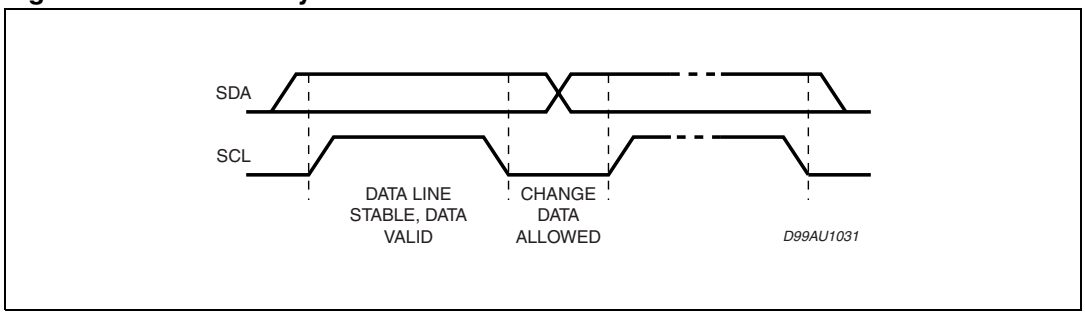


Figure 4. Timing diagram of I²C BUS

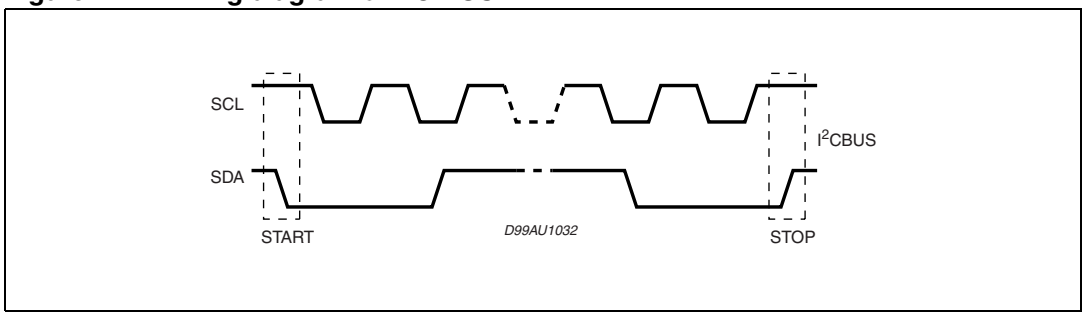
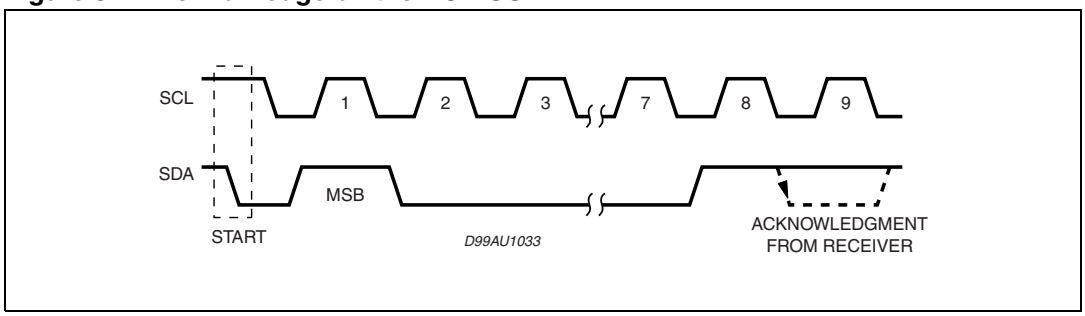


Figure 5. Acknowledge on the I²C BUS

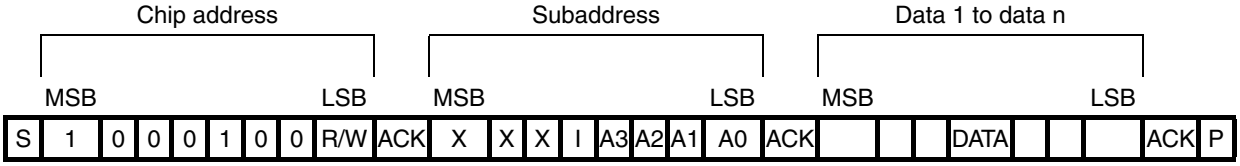


4 Software specification

4.1 Interface protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, (the LSB bit determines read/write transmission)
- A subaddress byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge

S = Start

P = Stop

I = Auto Increment

X = Not used

Max clock speed 500kbits/s

4.2 Auto increment

If bit I in the subaddress byte is set to "1", the auto-increment of the subaddress is enabled

Table 5. Subaddress (receive mode)

MSB							LSB	Function
X	X	X	I	A3	A2	A1	A0	
				0	0	0	0	Input selector
				0	0	0	1	Loudness
				0	0	1	0	Volume
				0	0	1	1	Bass, Treble
				0	1	0	0	Speaker attenuator LF
				0	1	0	1	Speaker attenuator LR
				0	1	1	0	Speaker attenuator RF
				0	1	1	1	Speaker attenuator RR
				1	0	0	0	Mute

4.3 Transmitted data

Table 6. Send mode

MSB							LSB
X	X	X	X	X	SM	ZM	X

ZM = Zero crossing muted (HIGH active)

SM = Soft mute activated (HIGH active)

X = Not used

The transmitted data is automatically updated after each ACK.

Transmission can be repeated without new chip address.

4.4 Data byte specification

X = not relevant; set to "1" during testing

Table 7. Input Selector

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	1			0	0	0	not used
X	X	1			0	0	1	IN 2
X	X	1			0	1	0	IN 1
X	X	1			0	1	1	AM mono
X	X	1			1	0	0	not used
X	X	1			1	0	1	IN 3
X	X	1			1	1	0	not allowed
X	X	1			1	1	1	not allowed
X	X	1	0	0				11.25dB gain
X	X	1	0	1				7.5dB gain
X	X	1	1	0				3.75dB gain
X	X	1	1	1				0dB gain

For example to select the IN 2 input with a gain of 7.5dB the Data Byte is: X X 1 0 1 0 0 1

Table 8. Loudness

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	1	0	0	0	0	0dB
X	X	X	1	0	0	0	1	-1.25dB
X	X	X	1	0	0	1	0	-2.5dB

Table 8. Loudness (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	1	0	0	1	1	-3.75dB
X	X	X	1	0	1	0	0	-5dB
X	X	X	1	0	1	0	1	-6.25dB
X	X	X	1	0	1	1	0	-7.5dB
X	X	X	1	0	1	1	1	-8.75dB
X	X	X	1	1	0	0	0	-10dB
X	X	X	1	1	0	0	1	-11.25dB
X	X	X	1	1	0	1	0	-12.5dB
X	X	X	1	1	0	1	1	-13.75dB
X	X	X	1	1	1	0	0	-15dB
X	X	X	1	1	1	0	1	-16.25dB
X	X	X	1	1	1	1	0	-17.5dB
X	X	X	1	1	1	1	1	-18.75dB

For example to select -17.5dB attenuation, loudness OFF, the Data Byte is: X X X1 1 1 1 0

Table 9. Mute

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
							1	Soft mute on
						0	1	Soft mute with fast slope (I = IMAX)
						1	1	Soft mute with slow slope (I = IMIN)
				1				Direct mute
			0		1			Zero crossing mute on
			0		0			Zero crossing mute off (delayed until next zerocrossing)
			1					Zero crossing mute and pause detector reset
	0	0						160mV ZC window threshold (WIN = 00)
	0	1						80mV ZC window threshold (WIN = 01)
	1	0						40mV ZC window threshold (WIN = 10)
	1	1						20mV ZC window threshold (WIN = 11)
0								Non-symmetrical Bass Cut
1								Symmetrical Bass Cut

An additional direct mute function is included in the speaker attenuators.

Note: Bass cut for very low frequencies should not be used at +16 & +18dB bass boost (DC gain)

Table 10. Speaker attenuators

MSB							LSB	Speaker attenuator LF, LR, RF, RR
D7	D6	D5	D4	D3	D2	D1	D0	
								1.25dB step
X	X	X			0	0	0	0dB
X	X	X			0	0	1	-1.25dB
X	X	X			0	1	0	-2.5dB
X	X	X			0	1	1	-3.75dB
X	X	X			1	0	0	-5dB
X	X	X			1	0	1	-6.25dB
X	X	X			1	1	0	-7.5dB
X	X	X			1	1	1	-8.75dB
								10dB step
X	X	X	0	0				0dB
X	X	X	0	1				-10dB
X	X	X	1	0				-20dB
X	X	X	1	1				-30dB
X	X	X	1	1	1	1	1	Speaker mute

For example an attenuation of 25dB on a selected output is given by: X X X1 0 1 0 0

Table 11. Bass/Treble

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Treble step
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB

Table 11. Bass/Treble (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB
								BASS STEPS
0	0	1	0					-10dB
0	0	1	1					-8dB
0	1	0	0					-6dB
0	1	0	1					-4dB
0	1	1	0					-2dB
0	1	1	1					-0dB
1	1	1	1					-0dB
1	1	1	0					2dB
1	1	0	1					4dB
1	1	0	0					6dB
1	0	1	1					8dB
1	0	1	0					10dB
1	0	0	1					12dB
1	0	0	0					14dB
0	0	0	1					146B
0	0	0	0					18dB

For example 12dB Treble and -8dB Bass give the following DATA BYTE: 0 0 1 1 1 0 0 1

Table 12. Volume

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								0.31dB Fine attenuation steps
						0	0	0dB
						0	1	-0.31dB
						1	0	-0.62dB
						1	1	-0.94dB
								1.25dB Coarse attenuation steps
			0	0	0			0dB
			0	0	1			-1.25dB
			0	1	0			-2.5dB
			0	1	1			-3.75dB
			1	0	0			-5dB
			1	0	1			-6.25dB
			1	1	0			-7.5dB
			1	1	1			-8.75dB
								10dB Gain / attenuation steps
0	0	0						20dB
0	0	1						10dB
0	1	0						0dB
0	1	1						-10dB
1	0	0						-20dB
1	0	1						-30dB
1	1	0						-40dB
1	1	1						-50dB

For example to select -47.81dB volume the data byte is: 1 1 0 1 1 0 0 1

Power on RESET: All bytes set to 1 1 1 1 1 1 1 0

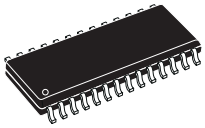
5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

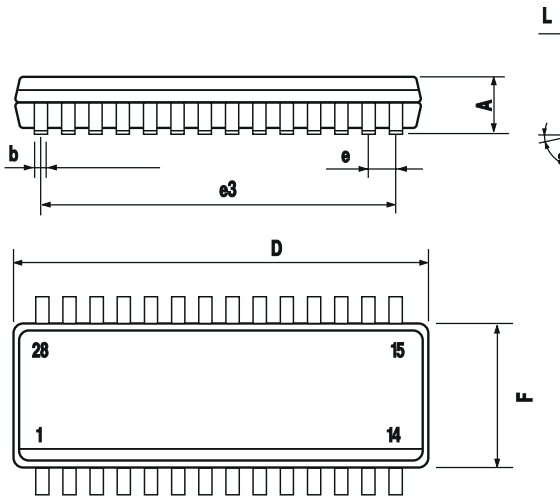
Figure 6. SO-28 mechanical, data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8 ° (max.)					

OUTLINE AND MECHANICAL DATA



SO-28



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
14-Jan-2004	1	Initial release.
21-Jun-2004	2	Technical migration from ST-PRESS to EDOCS DMS
26-Jan-2007	3	DIP28 package removed, block diagram changed, layout modified.

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