

Rail-to-rail CMOS quad operational amplifier

Features

- Rail-to-rail input and output voltage ranges
- Single (or dual) supply operation from 2.7V to 16V
- Extremely low input bias current: 1pA typ
- Low input offset voltage: 5mV max.
- Specified for 600Ω and 100Ω loads
- Low supply current: 200μA/ampli ($V_{CC} = 3V$)
- Latch-up immunity
- Spice macromodel included in this specification

Description

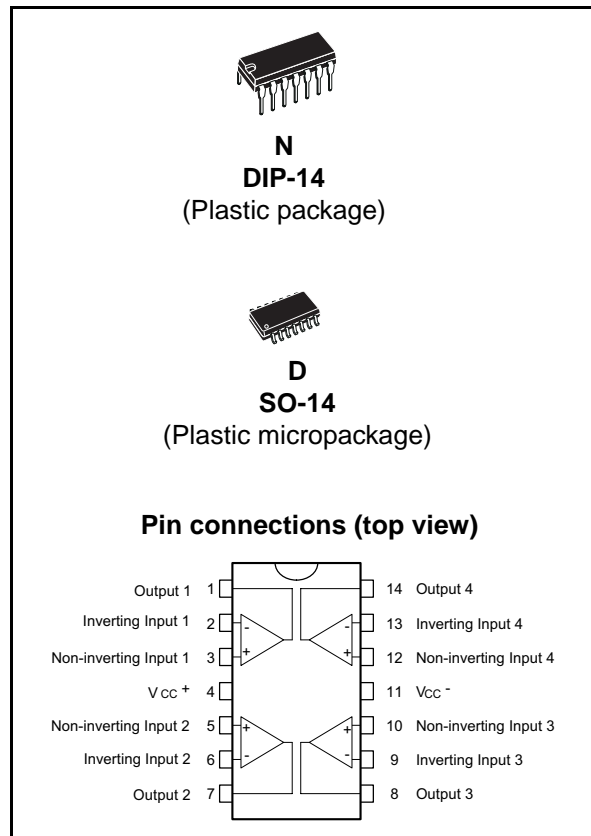
The TS914 is a rail-to-rail CMOS quad operational amplifier designed to operate with a single or dual supply voltage.

The input voltage range V_{icm} includes the two supply rails V_{CC}^+ and V_{CC}^- .

The output reaches:

- $V_{CC}^- + 50mV$, $V_{CC}^+ - 50mV$, with $R_L = 10k\Omega$
- $V_{CC}^- + 350mV$, $V_{CC}^+ - 350mV$, with $R_L = 600\Omega$

This product offers a broad supply voltage operating range from 2.7V to 16V and a supply current of only 200μA/amp ($V_{CC} = 3V$).



Source and sink output current capability is typically 40mA (at $V_{CC} = 3V$), fixed by an internal limitation circuit.

Order codes

Part number	Temperature range	Package	Packing	Marking
TS914IN	-40, +125°C	DIP14	Tube	TS914IN
TS914ID/IDT		SO-14	Tube or tape & reel	914I
TS914AIN		DIP14	Tube	TS914AIN
TS914AID/AIDT		SO-14	Tube or tape & reel	914AI
TS914IYD/IYDT		SO-14 (automotive grade level)	Tube or tape & reel	914IY
TS914AIYD/AIYDT				914AIY

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1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Test conditions	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾		18	V
V_{id}	Differential input voltage ⁽²⁾		± 18	V
V_i	Input voltage ⁽³⁾		-0.3 to 18	V
I_{in}	Current on inputs		± 50	mA
I_o	Current on outputs		± 130	mA
T_j	Maximum junction temperature		150	°C
T_{stg}	Storage temperature		-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient ⁽⁴⁾	DIP-14	83	°C/W
		SO-14	103	
R_{thjc}	Thermal resistance junction to case	DIP-14	33	°C/W
		SO-14	31	
ESD	HBM: human body model ⁽⁵⁾		1	kV
	MM: machine model ⁽⁶⁾		50	V
	CDM: charged device model ⁽⁷⁾		1.5	kV

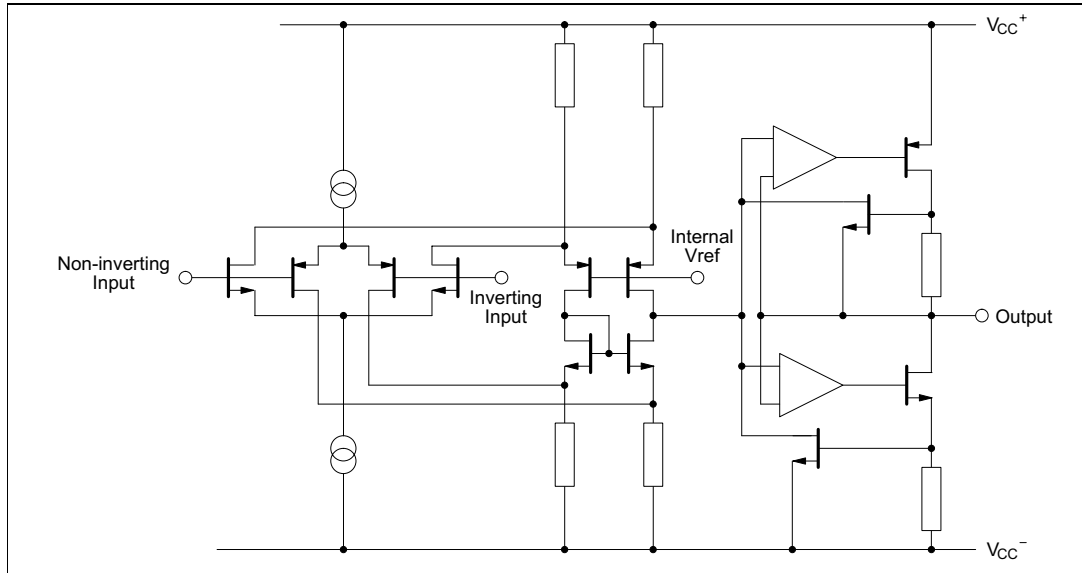
1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed $V_{CC}^+ + 0.3V$.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuit on all amplifiers. These are typical values.
5. Human body model: A 100pF capacitor is charged to the specified voltage, then discharged through a 1.5k Ω resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: A 200pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 16	V
V_{icm}	Common mode input voltage range	$V_{CC}^- - 0.2$ to $V_{CC}^+ + 0.2$	V
T_{oper}	Operating free air temperature range	-40 to + 125	°C

2 Typical application information

Figure 1. Typical application information



3 Electrical characteristics

Table 3. $V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, R_L , C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_{icm} = V_o = V_{CC}/2$)	T_{amb} TS914 T_{amb} TS914A $T_{min} \leq T_{amb} \leq T_{max}$, TS914 $T_{min} \leq T_{amb} \leq T_{max}$, TS914A			10 5 12 7	mV
ΔV_{io}	Input offset voltage drift			5		$\mu V/^\circ C$
I_{io}	Input offset current ⁽¹⁾	T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$		1	100 200	pA
I_{ib}	Input bias current ⁽¹⁾	T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$		1	150 300	pA
I_{CC}	Supply current	per amplifier, $A_{VCL} = 1$, no load T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$		200	300 400	μA
CMR	Common mode rejection ratio	$V_{ic} = 0$ to $3V$, $V_o = 1.5V$		70		dB
SVR	Supply voltage rejection ratio	$V_{CC}^+ = 2.7$ to $3.3V$, $V_o = V_{CC}/2$		80		dB
A_{vd}	Large signal voltage gain	$R_L = 10k\Omega$, $V_o = 1.2V$ to $1.8V$ T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$	3 2	10		V/mV
V_{OH}	High level output voltage	$V_{id} = 1V$, T_{amb} $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $V_{id} = 1V$, $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$	2.9 2.2	2.97 2.7 2		V
V_{OL}	Low level output voltage	$V_{id} = -1V$, T_{amb} $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $V_{id} = -1V$, $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$		50 300 900	100 600	mV
I_o	Output short circuit current	$V_{id} = \pm 1V$ Source ($V_o = V_{CC}$) Sink ($V_o = V_{CC}^+$)		40 40		mA
GBP	Gain bandwidth product	$A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, $f = 100kHz$		0.8		MHz
SR	Slew rate	$A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 1.3V$ to $1.7V$		0.5		V/ μs
ϕ_m	Phase margin			30		$^\circ$
e_n	Equivalent input noise voltage	$R_s = 100\Omega$, $f = 1kHz$		30		nV/ \sqrt{Hz}
V_{O1}/V_{O2}	Channel separation	$f = 1kHz$		120		dB

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 4. $V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, R_L , C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_{icm} = V_o = V_{CC}/2$)	T_{amb} , TS914 T_{amb} , TS914A $T_{min} \leq T_{amb} \leq T_{max}$, TS914 $T_{min} \leq T_{amb} \leq T_{max}$, TS914A			10 5 12 7	mV
ΔV_{io}	Input offset voltage drift			5		$\mu V/^\circ C$
I_{io}	Input offset current (1)	T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$		1	100 200	pA
I_{ib}	Input bias current (1)	T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$		1	150 300	pA
I_{CC}	Supply current	per amplifier, $A_{VCL} = 1$, no load T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$		230	350 450	μA
CMR	Common mode rejection ratio	$V_{ic} = 1.5$ to $3V$, $V_o = 2.5V$		85		dB
SVR	Supply voltage rejection ratio	$V_{CC}^+ = 3$ to $5V$, $V_o = V_{CC}/2$		80		dB
A_{vd}	Large signal voltage gain	$R_L = 10k\Omega$, $V_o = 1.5V$ to $3.5V$ T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$	10 7	40		V/mV
V_{OH}	High level output voltage	$V_{id} = 1V$, T_{amb} $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $V_{id} = 1V$, $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$	4.85 4.20	4.95 4.65 3.7		V
V_{OL}	Low level output voltage	$V_{id} = -1V$, T_{amb} $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $V_{id} = -1V$, $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$		50 350 1400	100 680	mV
I_o	Output short circuit current	$V_{id} = \pm 1V$ Source ($V_o = V_{CC}$) Sink ($V_o = V_{CC}^+$)		60 60		mA
GBP	Gain bandwidth product	$A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, $f = 100kHz$		1		MHz
SR	Slew rate	$A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 1V$ to $4V$		0.8		V/ μs
ϕ_m	Phase margin			30		$^\circ$
e_n	Equivalent input noise voltage	$R_s = 100\Omega$, $f = 1kHz$		30		nV/ \sqrt{Hz}
V_{O1}/V_{O2}	Channel separation	$f = 1kHz$		120		dB

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Table 5. $V_{CC^+} = 10V$, $V_{DD} = 0V$, R_L , C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_{icm} = V_o = V_{CC}/2$)	T_{amb} , TS914 T_{amb} , TS914A $T_{min} \leq T_{amb} \leq T_{max}$, TS914 $T_{min} \leq T_{amb} \leq T_{max}$, TS914A			10 5 12 7	mV
ΔV_{io}	Input offset voltage drift			5		$\mu V/^\circ C$
I_{io}	Input offset current ⁽¹⁾	T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$		1	100 200	pA
I_{ib}	Input bias current ⁽¹⁾	T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$		1	150 300	pA
V_{icm}	Common mode input voltage range	Per amplifier, $A_{VCL} = 1$, no load T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$	$V_{DD} - 0.2$ to $V_{CC} + 0.2$			V
CMR	Common mode rejection ratio	$V_{ic} = 3$ to $7V$, $V_o = 5V$ $V_{ic} = 0$ to $10V$, $V_o = 5V$		90 75		dB
SVR	Supply voltage rejection ratio	$V_{CC^+} = 5$ to $10V$, $V_o = V_{CC}/2$		90		dB
A_{vd}	Large signal voltage gain	$R_L = 10k\Omega$, $V_o = 2.5V$ to $7.5V$ T_{amb} $T_{min} \leq T_{amb} \leq T_{max}$	15 10	60		V/mV
V_{OH}	High level output voltage	$V_{id} = 1V$, T_{amb} $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $V_{id} = 1V$, $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$	9.85 9 9.8 9	9.95 9.35 7.8		V
V_{OL}	Low level output voltage	$V_{id} = -1V$, T_{amb} $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $V_{id} = -1V$, $T_{min} \leq T_{amb} \leq T_{max}$ $R_L = 10k\Omega$ $R_L = 600\Omega$		50 650 2300	180 800	mV
I_o	Output short circuit current	$V_{id} = \pm 1V$		60		mA
I_{CC}	Supply current	Per amplifier, $A_{VCL} = 1$, no load, T_{amb} Per amp., $A_{VCL} = 1$, no load, $T_{min} \leq T_{amb} \leq T_{max}$		400	600 700	μA
GBP	Gain bandwidth product	$A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, $f = 100kHz$		1.4		MHz
SR	Slew rate	$A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 2.5V$ to $7.5V$		1		V/ μs
ϕ_m	Phase margin	$R_s = 100\Omega$, $f = 1kHz$		40		$^\circ$
e_n	Equivalent input noise voltage	$R_s = 100\Omega$, $f = 1kHz$		30		nV/ \sqrt{Hz}

Table 5. $V_{CC^+} = 10V$, $V_{DD} = 0V$, R_L , C_L connected to $V_{CC}/2$, $T_{amb} = 25^{\circ}C$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
THD	Total harmonic distortion	$A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_o = 4.75$ to $5.25V$, $f = 1kHz$		0.02		%
C_{in}	Input capacitance			1.5		pF
R_{in}	Input resistance			>10		Tera Ω
V_{O1}/V_{O2}	Channel separation	$f = 1kHz$		120		dB

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Figure 2. Supply current (each amplifier) vs. supply voltage

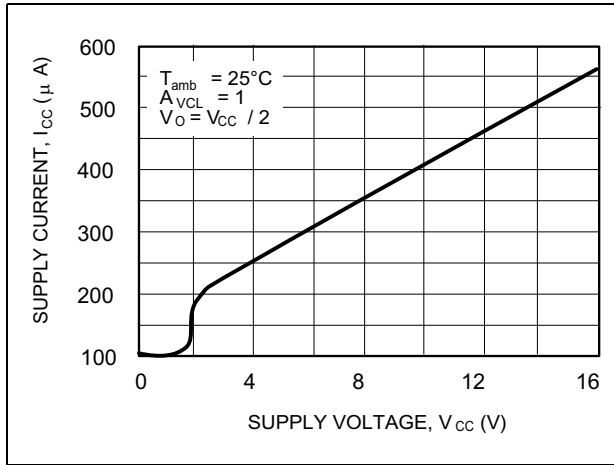


Figure 3. High level output voltage vs. high level output current

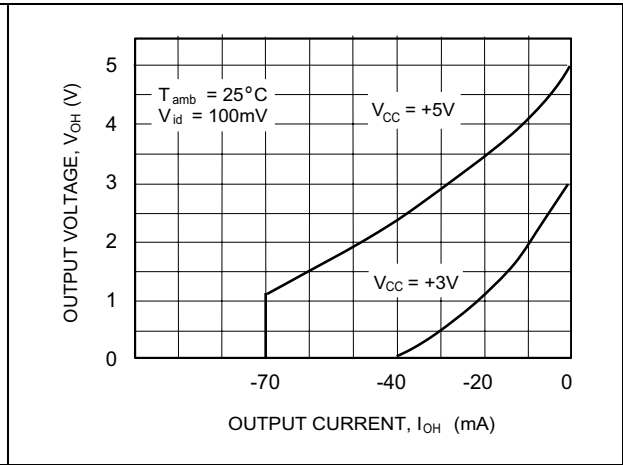


Figure 4. Low level output voltage vs. low level output current

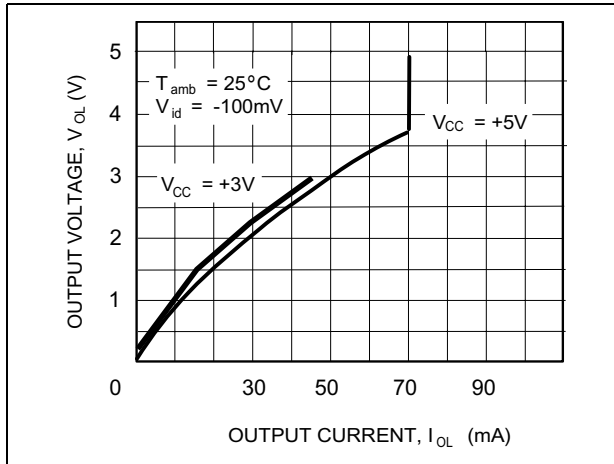


Figure 5. Input bias current vs. temperature

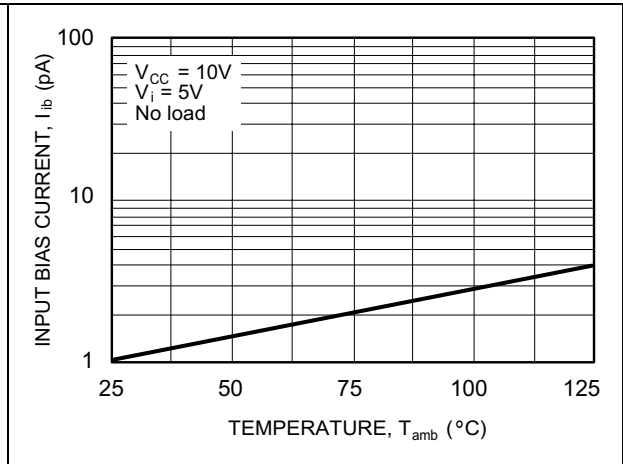


Figure 6. High level output voltage vs. high level output current

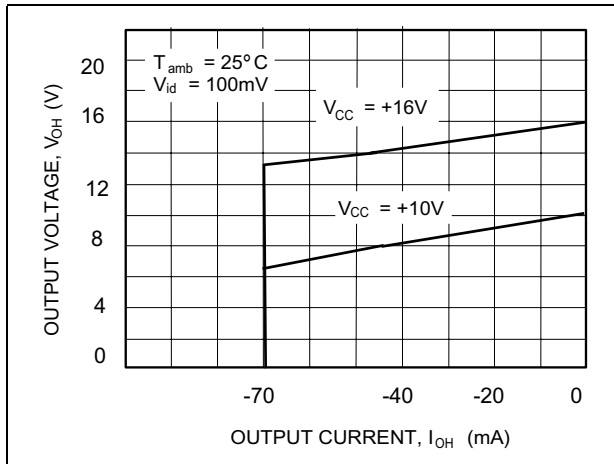


Figure 7. Low level output voltage vs. low level output current

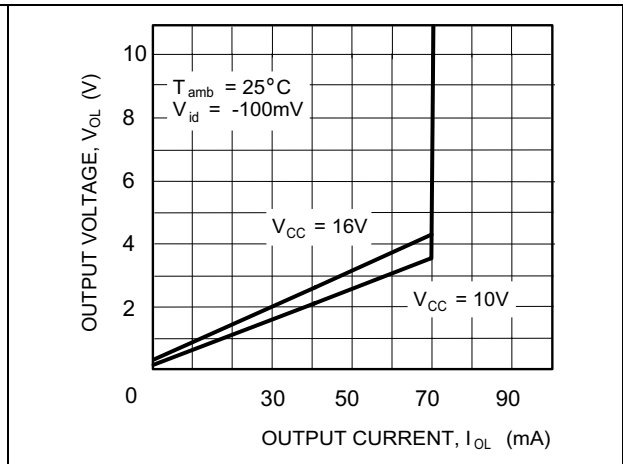


Figure 8. Gain and phase vs. frequency

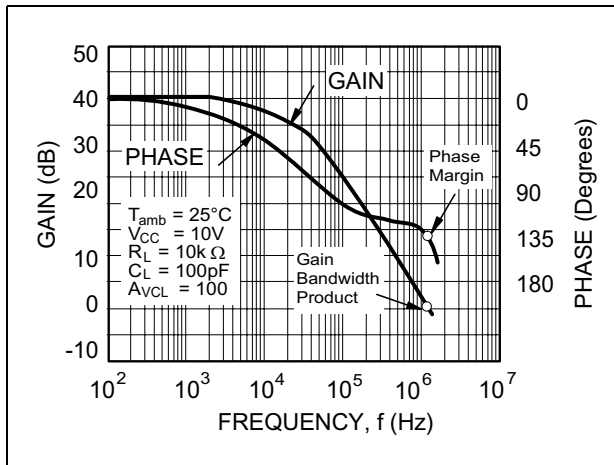


Figure 9. Gain bandwidth product vs. supply voltage

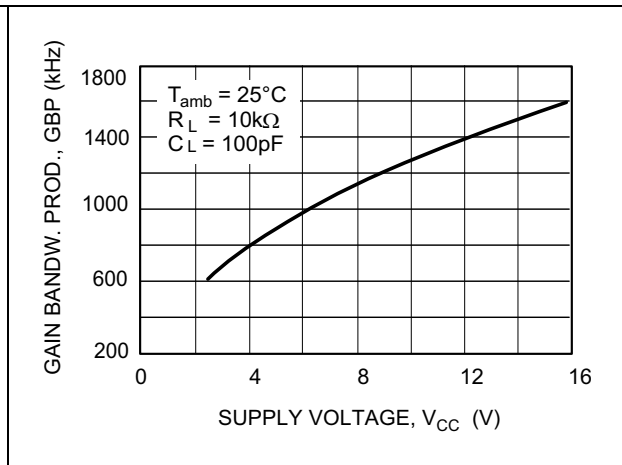


Figure 10. Phase margin vs. supply voltage

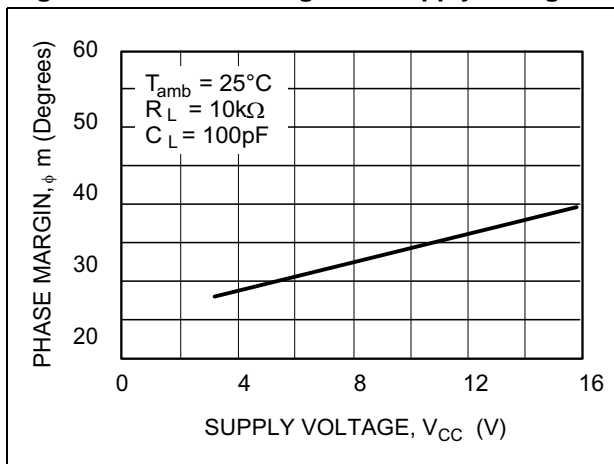


Figure 11. Gain and phase vs. frequency

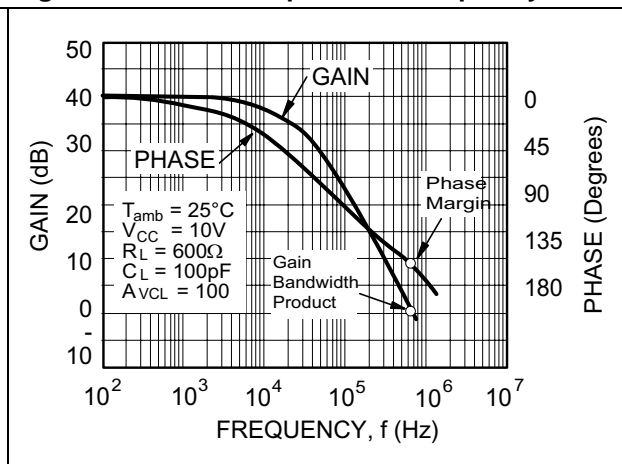


Figure 12. Gain bandwidth product vs. supply voltage

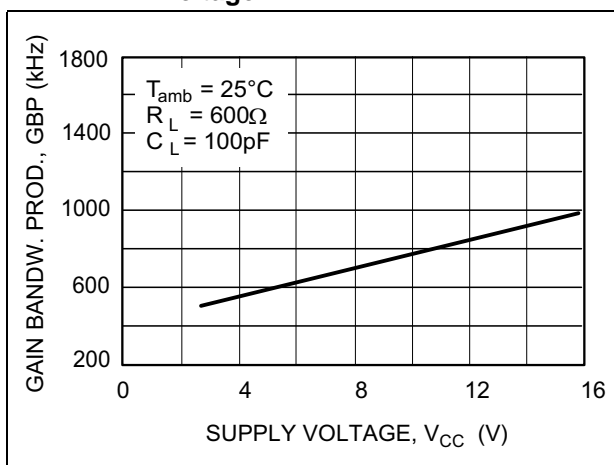


Figure 13. Phase margin vs. supply voltage

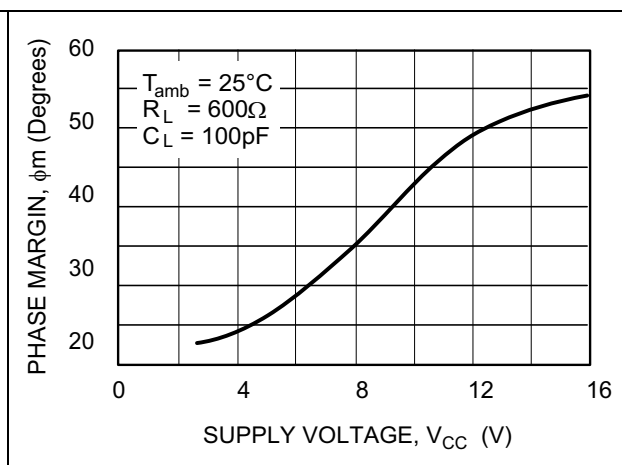
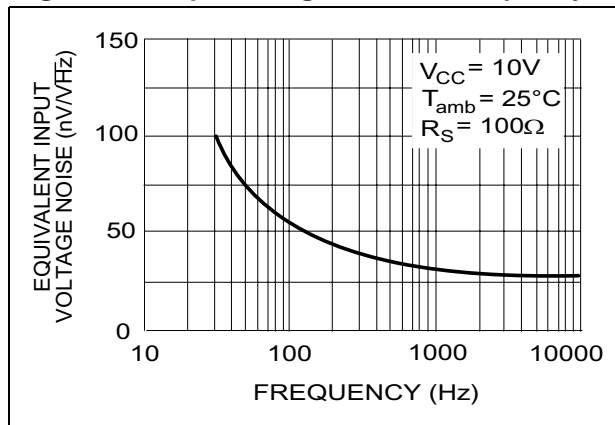


Figure 14. Input voltage noise vs. frequency

4 Macromodels

4.1 Important note concerning this macromodel

Please consider the following remarks before using this macromodel:

- All models are a trade-off between accuracy and complexity (i.e. simulation time). Macromodels are not a substitute for breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the **nominal** performance of a **typical** device within **specified operating conditions** (such as temperature or supply voltage, etc). Thus, the macromodel is often not as exhaustive as the datasheet, its purpose is to illustrate the main parameters of the product.
- Data derived from macromodels used outside of the specified conditions (such as V_{CC} , or temperature) or even worse, outside of the device's operating conditions (such as V_{CC} or V_{icm}) is not reliable in any way.

The values provided in [Table 6](#) are derived from this macromodel.

Table 6. $V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, R_L , C_L connected to $V_{CC}/2$, $T_{amb} = 25^\circ C$ (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	$R_L = 10k\Omega$	10	V/mV
I_{CC}	No load, per operator	100	μA
V_{icm}		-0.2 to 3.2	V
V_{OH}	$R_L = 600\Omega$	2.96	V
V_{OL}	$R_L = 60\Omega$	300	mV
I_{sink}	$V_O = 3V$	40	mA
I_{source}	$V_O = 0V$	40	mA
GBP	$R_L = 10k\Omega$, $C_L = 100pF$	0.8	MHz
SR	$R_L = 10k\Omega$, $C_L = 100pF$	0.3	V/ μs
ϕ_m	Phase margin	30	Degrees

4.2 Macromodel code

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* Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
*
.SUBCKT TS914 1 2 3 4 5
*****
.MODEL MDTH D IS=1E-8 KF=6.564344E-14 CJO=10F
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 6.500000E+00
RIN 15 16 6.500000E+00
RIS 11 15 7.322092E+00
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0.000000E+00
VOFN 13 14 DC 0
IPOL 13 5 4.000000E-05
CPS 11 15 2.498970E-08
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000E+00
DINR 15 18 MDTH 400E-12
VIP 4 18 0.000000E+00
FCP 4 5 VOFP 5.750000E+00
FCN 5 4 VOFN 5.750000E+00
* AMPLIFYING STAGE
FIP 5 19 VOFP 4.400000E+02
FIN 5 19 VOFN 4.400000E+02
RG1 19 5 4.904961E+05
RG2 19 4 4.904961E+05
CC 19 29 2.200000E-08
HZTP 30 29 VOFP 1.8E+03
HZTN 5 30 VOFN 1.8E+03
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 3800
VIPM 28 4 230
HONM 21 27 VOUT 3800
VINM 5 27 230
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 82
COUT 3 5 1.000000E-12
DOP 19 68 MDTH 400E-12
VOP 4 25 1.724

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HSCP 68 25 VSCP1 0.8E+8
DON 69 19 MDTH 400E-12
VON 24 5 1.7419107
HSCN 24 69 VSCN1 0.8E+8
VSCTHP 60 61 0.0875
DSCP1 61 63 MDTH 400E-12
VSCP1 63 64 0
ISCP 64 0 1.000000E-8
DSCP2 0 64 MDTH 400E-12
DSCN2 0 74 MDTH 400E-12
ISCN 74 0 1.000000E-8
VSCN1 73 74 0
DSCN1 71 73 MDTH 400E-12
VSCTHN 71 70 -0.55
ESCP 60 0 2 1 500
ESCN 70 0 2 1 -2000
.ENDS
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5 Package mechanical data

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

5.1 DIP-14 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

The figure contains three mechanical drawings of the DIP-14 package. The top-left drawing is a side view showing the package profile with dimensions: a1 (lead height), B (lead width), b (lead thickness), b1 (lead thickness at base), e (pitch), e3 (total length), F (lead length), l (lead length), and Z (lead thickness). The top-right drawing is a perspective view showing dimensions b1 and E (package width). The bottom drawing is a top view showing dimensions D (package length) and F (package height), and pin numbers 1, 7, 8, and 14.

5.2 SO-14 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					
<p>The figure contains three mechanical drawings of the SO-14 package. The top-left drawing is a side view showing dimensions A (total height), a2 (lead height), b (lead width), e (pitch), and e3 (total length). The top-right drawing is a perspective view showing dimensions L (lead length), G (lead width), C (lead thickness), c1 (lead angle), a1 (lead thickness), b1 (lead width), and F (package width). The bottom drawing is a top view showing dimensions D (total length), M (lead length), and F (package width), with pin numbers 1, 7, 8, and 14 indicated.</p>						

6 Revision history

Date	Revision	Changes
1-Dec-2001	1	First release.
1-Nov-2004	2	V_{io} max on 1st page from 2mV to 5mV.
1-Jun-2005	3	PIPAP references inserted in the datasheet see order code table on cover page.
1-Feb-2006	4	Parameters added in Table 1. on page 3 (T_j , ESD, R_{thja} , R_{thjc}).
8-Jan-2007	5	Correction to package name in order code table on cover page. Addition of a table of contents. Corrections to macromodel.

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