SN10KHT5574 OCTAL ECL-TO-TTL TRANSLATOR WITH D-TYPE EDGE-TRIGGERED FLIP-FLOPS AND 3-STATE OUTPUTS

SDZS010 - JANUARY 1990 - REVISED OCTOBER 1990

- 10KH Compatible
- ECL Clock and TTL Control Inputs
- Flow-Through Architecture Optimizes PCB Layout
- Center Pin V_{CC}, V_{EE}, and GND Configurations Minimize High-Speed Switching Noise
- Package Options Include "Small Outline" Packages and Standard Plastic DIPs

description

This octal ECL-to-TTL translator is designed to provide efficient translation between a 10KH ECL signal environment and a TTL signal environment.

This device is designed specifically to improve the performance and density of ECL-to-TTL CPU/bus-oriented functions such as memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The eight flip-flops of the SN10KHT5574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels that were set up at the D inputs.

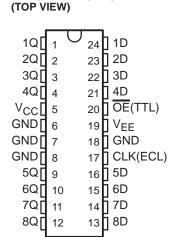
A buffered output-enable input (\overline{OE}) can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance third state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable input $\overline{\text{OE}}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN10KHT5574 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

l II	NPUTS	OUTPUT (TTL)	
ŌĒ	CLK	D	Q
L	1	Г	L
L	\uparrow	Н	Н
L	L	Χ	Qo
Н	Χ	Χ	Z

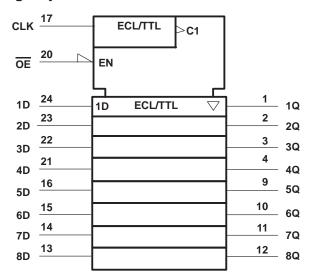


DW OR NT PACKAGE



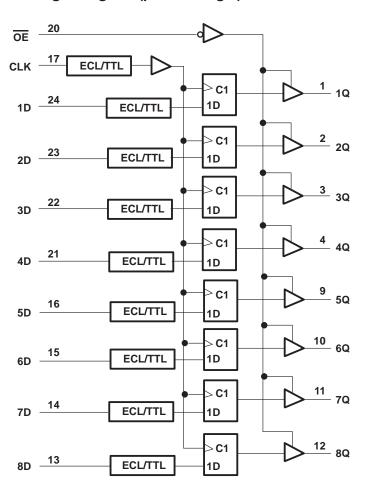
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logic symbol†



 $[\]ensuremath{^{\dagger}}$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	0.5 V to 7 V
Supply voltage range, V _{EE}	8 V to 0 V
Input voltage range: TTL (see Note 1)	1.2 V to 7 V
ECL	V _{EE} to 0 V
Voltage applied to any output in the disabled or power-off state	0.5 V to 5.5 V
Voltage applied to any output in the high state	0.5 V to V _{CC}
Input current range, (TTL)	30 mA to 5 mA
Current into any output in the low state	96 mA
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The TTL input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
VCC	V _{CC} TTL supply voltage				5.5	V
VEE	ECL supply voltage		-4.94	-5.2	-5.46	V
VIH	TTL high-level input voltage		2			V
V _{IL}	TTL low-level input voltage				0.8	V
		T _A = 0°C	-1170		-840	
VIH ECL high-level in	ECL high-level input voltage‡	T _A = 25°C	-1130		-810	mV
		T _A = 75°C	-1070		-735	
		T _A = 0°C	-1950		-1480	mV
VIL	ECL low-level input voltage [‡]	T _A = 25°C	-1950		-1480	
		T _A = 75°C	-1950		-1450	
lik	I _{IK} TTL input clamp current				-18	mA
ГОН	OH High-level output current				-15	mA
loL	DL Low-level output current				48	mA
TA					75	°C

[‡]The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic levels only.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	6		MIN	TYP [†]	MAX	UNIT
٧ıK	OE only	$V_{CC} = 4.5 \text{ V},$	$V_{EE} = -4.94 \text{ V},$	$I_{I} = -18 \text{ mA}$				-1.2	V
VOH	$V_{CC} = 4.5 \text{ V},$	$V_{EE} = -5.2 \text{ V} \pm 5\%$,	$I_{OH} = -3 \text{ mA}$		2.4	3.3		V	
VOH		$V_{CC} = 4.5 \text{ V},$	$V_{EE} = -5.2 \text{ V} \pm 5\%$,	$I_{OH} = -15 \text{ mA}$		2	3.1		V
VOL		$V_{CC} = 4.5 \text{ V},$	$V_{EE} = -5.2 \text{ V} \pm 5\%$,	$I_{OL} = 48 \text{ mA}$			0.38	0.55	V
IJ	OE only		$V_{EE} = -5.46 \text{ V},$	V _I = 7 V				0.1	mA
lн	OE only	$V_{CC} = 5.5 \text{ V},$	$V_{EE} = -5.46 \text{ V},$	V _I = 2.7 V				20	μΑ
Ι _Ι L	OE only	$V_{CC} = 5.5 \text{ V},$	$V_{EE} = -5.46 \text{ V},$	V _I = 0.5 V				-0.5	mA
		$V_{CC} = 5.5 \text{ V},$	$V_{EE} = -5.46 \text{ V},$	$V_{I} = -840 \text{ mV}$	T _A = 0°C			350	
lіН	Data inputs and CLK	$V_{CC} = 5.5 \text{ V},$	$V_{EE} = -5.46 \text{ V},$	$V_{I} = -810 \text{ mV}$	T _A = 25°C			350	μΑ
		$V_{CC} = 5.5 \text{ V},$	$V_{EE} = -5.46 \text{ V},$	$V_{I} = -735 \text{ mV}$	T _A = 75°C			350	
					$T_A = 0^{\circ}C$	0.5			
IJL	Data inputs and CLK	$V_{CC} = 5.5 V$,	$V_{EE} = -5.46 \text{ V},$	$V_{I} = -1950 \text{ mV}$	T _A = 25°C	0.5			μΑ
					T _A = 75°C	0.5			
lozh		$V_{CC} = 5.5 \text{ V},$	$V_{EE} = -5.46 \text{ V},$	V _O = 2.7 V				50	μΑ
lozL		$V_{CC} = 5.5 \text{ V},$	$V_{EE} = -5.46 \text{ V},$	$V_0 = 0.5 V$				-50	μΑ
los‡		$V_{CC} = 5.5 \text{ V},$	$V_{EE} = -5.46 \text{ V},$	V _O = 0 V		-100		-225	mA
ICCH		$V_{CC} = 5.5 \text{ V},$	V _{EE} = -5.46 V				66	95	mA
ICCL		$V_{CC} = 5.5 \text{ V},$	V _{EE} = −5.46 V				76	110	mA
ICCZ		$V_{CC} = 5.5 \text{ V},$	$V_{EE} = -5.46 \text{ V}$				74	106	mA
IEE		$V_{CC} = 5.5 V$,	V _{EE} = -5.46 V				-43	-61	mA
Ci		$V_{CC} = 5.5 \text{ V},$	V _{EE} = −5.2 V,	f = 10 MHz			5		рF
Co		$V_{CC} = 5.5 \text{ V},$	$V_{EE} = -5.2 \text{ V},$	f = 10 MHz			7		pF

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $V_{EE} = -5.2 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements

			$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $V_{EE} = -4.94 \text{ V to } -5.46 \text{ V},$ $T_A = MIN \text{ to } MAX$ §	UNIT
			MIN MA	(
	t _W Pulse duration	CLK high	4	
I _W		CLK low	4	ns
	0.44.5 (2.5.4 h.s/s 01.1/1	Data high	1	
tsu	Setup time before CLK↑	Data low	1	ns
th	Hold time after CLK↑	Data high	1	
41	Tiold time after OLIV	Data low	1	ns

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

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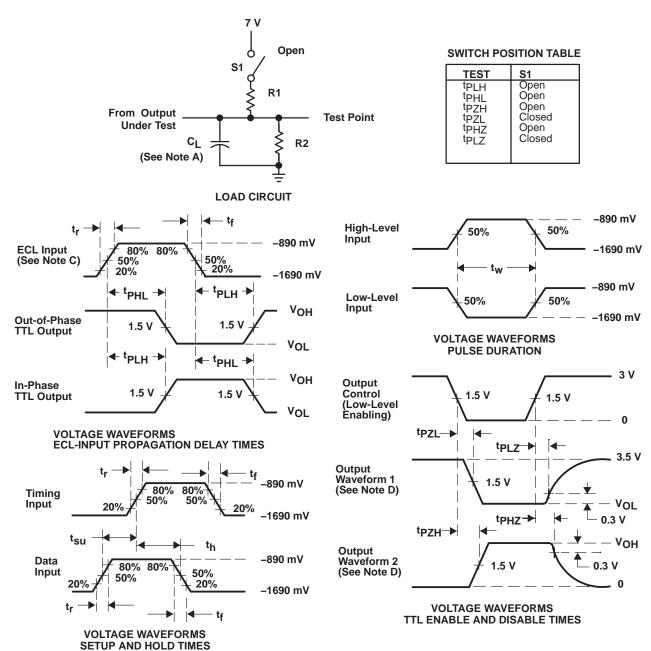
switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	R′	L = 50 pF 1 = 500 Ω 2 = 500 Ω	2,	UNIT
			MIN	TYP [†]	MAX	
f _{max}			200	300		MHz
t _{PLH}	CLIV	•	2.3	4.1	7	
^t PHL	CLK	Q	2.9	4.6	7.4	ns
^t PZH	ŌĒ	Q	1.9	3.6	6.3	no
t _{PZL}	OE .	3	2.7	4.8	7.7	ns
^t PHZ	ŌĒ	0	2.1	3.9	6.1	20
tPLZ	OE .	Q	0.5	3.4	6.3	ns

 $[\]dagger$ All typical values are at V_{CC} = 5 V, V_{EE} = -5.2 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION



NOTES: A.C_I includes probe and jig capacitance.

- B. For TTL inputs, input pulses are supplied by generators having the following characteristics PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \le 2.5 \text{ ns.}$
- C. For ECL inputs, input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_0 = 50 \Omega$, $t_r \leq 1.5 \text{ ns}$, $t_f \le 1.5 \text{ ns.}$
- D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load circuit and voltage waveforms







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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN10KHT5543DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN10KHT5543DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN10KHT5543DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN10KHT5543DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN10KHT5543NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN10KHT5543NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN10KHT5574DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN10KHT5574DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
SN10KHT5574NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN10KHT5574NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

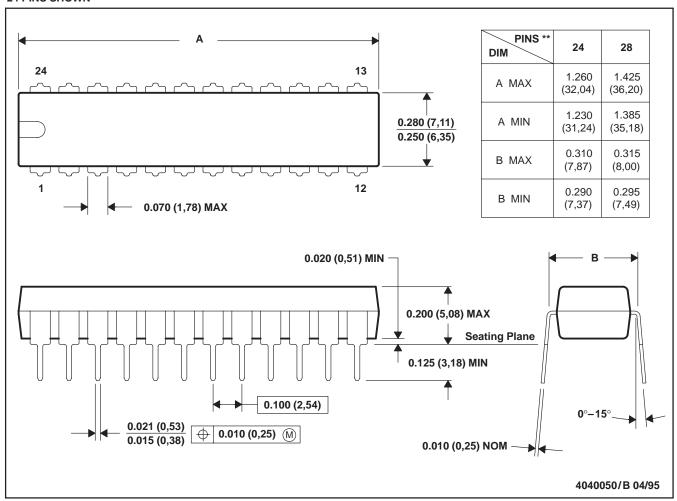
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NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN

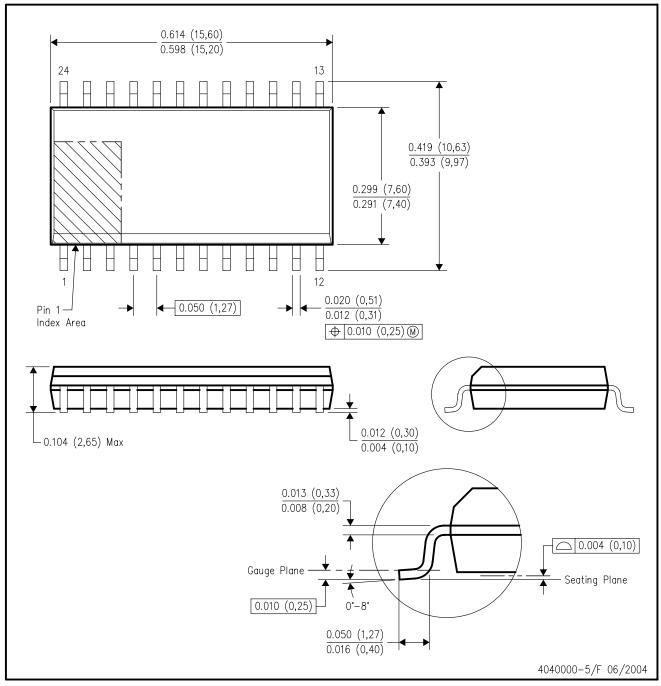


NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.



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