



## HIGH OUTPUT FULL-DUPLEX RS-485 DRIVERS AND RECEIVERS

### FEATURES

- 1/8 Unit-Load Option Available (Up to 256 Nodes on the Bus)
- Bus-Pin ESD Protection Exceeds 15 kV HBM
- Optional Driver Output Transition Times for Signaling Rates<sup>(1)</sup> of 1 Mbps, 5 Mbps and 25 Mbps
- Low-Current Standby Mode < 1  $\mu$ A
- Glitch-Free Power-Up and Power-Down Bus I/Os
- Bus Idle, Open, and Short Circuit Failsafe
- Designed for RS-422 and RS485 Networks
- 3.3-V Devices Available, SN65HVD30-39

<sup>(1)</sup> The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

### APPLICATIONS

- Utility Meters
- Chassis-to-Chassis Interconnects
- DTE/DCE Interfaces
- Industrial, Process, and Building Automation
- Point-of-Sale (POS) Terminals and Networks

### DESCRIPTION

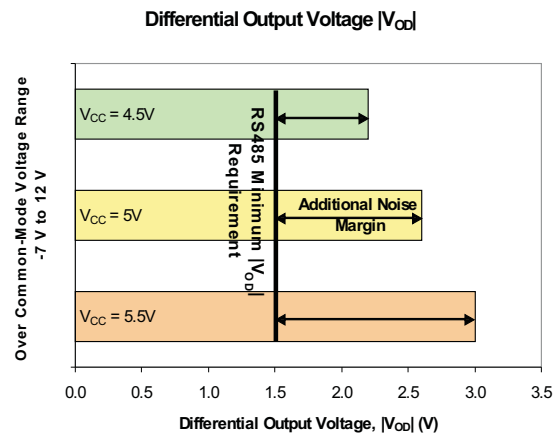
The SN65HVD5X devices are 3-state differential line drivers and differential-input line receivers that operate with a 5-V power supply. Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for balanced transmission lines and interoperability with ANSI TIA/EIA-485A, TIA/EIA-422-B, ITU-T v.11 and ISO 8482:1993 standard-compliant devices.

The SN65HVD50, SN65HVD51, SN65HVD52, SN65HVD56 and SN65HVD57 are fully enabled with no external enabling pins.

The SN65HVD53, SN65HVD54, SN65HVD55, SN65HVD58, and SN65HVD59 have active-high driver enables and active-low receiver enables. A low, less than 1  $\mu$ A, standby current is achieved by disabling both the driver and receiver.

All devices are characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

The high output feature of the SN65HVD5x provides more noise margin than the typical RS-485 drivers. The extra noise margin makes applications in long cable and harsh noise environments possible.



The SN65HVD56 and SN65HVD58 implement receiver equalization technology for improved jitter performance on differential bus applications with data rates up to 20 Mbps at cable lengths up to 160 meters.

The SN65HVD57 and SN65HVD59 implement receiver equalization technology for improved jitter performance on differential bus applications with data rates in the range of 1 to 5 Mbps at cable lengths up to 1000 meters.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN65HVD50-SN65HVD59

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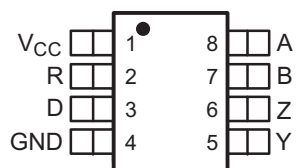
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

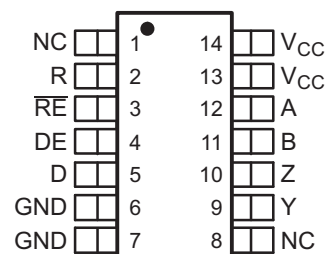
## SN65HVD50, SN65HVD51, SN65HVD52, SN65HVD56, SN65HVD57

D PACKAGE (TOP VIEW)

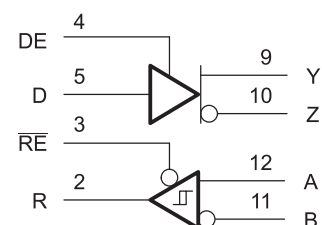


## SN65HVD53, SN65HVD54, SN65HVD55, SN65HVD58, SN65HVD59

D PACKAGE (TOP VIEW)



NC - No internal connection



### AVAILABLE OPTIONS

SIGNALING RATE	UNIT LOADS	RECEIVER EQUALIZATION	ENABLES	BASE PART NUMBER	SOIC MARKING
25 Mbps		No	No	SN65HVD50	65HVD50
5 Mbps	1/8	No	No	SN65HVD51	65HVD51
1 Mbps	1/8	No	No	SN65HVD52	65HVD52
25 Mbps		No	Yes	SN65HVD53	65HVD53
5 Mbps	1/8	No	Yes	SN65HVD54	65HVD54
1 Mbps	1/8	No	Yes	SN65HVD55	65HVD55
25 Mbps		Yes	No	SN65HVD56	PREVIEW
5 Mbps	1/8	Yes	No	SN65HVD57	PREVIEW
25 Mbps		Yes	Yes	SN65HVD58	PREVIEW
5 Mbps	1/8	Yes	Yes	SN65HVD59	PREVIEW

## ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		UNIT
$V_{CC}$	Supply voltage range	-0.3 V to 6 V
$V_{(A)}, V_{(B)}, V_{(Y)}, V_{(Z)}$	Voltage range at any bus terminal (A, B, Y, Z)	-9 V to 14 V
$V_{(TRANS)}$	Voltage input, transient pulse through 100 $\Omega$ . See <a href="#">Figure 12</a> (A, B, Y, Z) <sup>(3)</sup>	-50 to 50 V
$V_I$	Voltage input range (D, DE, $\overline{RE}$ )	-0.5 V to 7 V
$P_{D(cont)}$	Continuous total power dissipation	Internally limited <sup>(4)</sup>
$I_O$	Output current (receiver output only, R)	11 mA

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) This tests survivability only and the output state of the receiver is not specified.
- (4) The thermal shutdown typically occurs when the junction temperature reaches 165°C.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		4.5		5.5	V
$V_I$ or $V_{IC}$	Voltage at any bus terminal (separately or common mode)		-7 <sup>(1)</sup>		12	
$1/t_{UI}$	Signaling rate	SN65HVD50, SN65HVD53, SN65HVD56, SN65HVD58			25	Mbps
		SN65HVD51, SN65HVD54, SN65HVD57, SN65HVD59			5	
		SN65HVD52, SN65HVD55			1	
$R_L$	Differential load resistance		54	60		$\Omega$
$V_{IH}$	High-level input voltage	D, DE, $\overline{RE}$	2		$V_{CC}$	V
$V_{IL}$	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	
$V_{ID}$	Differential input voltage		-12		12	
$I_{OH}$	High-level output current	Driver	-60			mA
		Receiver	-8			
$I_{OL}$	Low-level output current	Driver			60	mA
		Receiver			8	
$T_J$ <sup>(2)</sup>	Junction temperature		-40		150	°C

- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
- (2) See thermal characteristics table for information regarding this specification.

## ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
Human body model	Bus terminals and GND		$\pm 16$		kV
Human body model <sup>(2)</sup>	All pins		$\pm 4$		
Charged-device-model <sup>(3)</sup>	All pins		$\pm 1$		

- (1) All typical values at 25°C and with a 5-V supply.
- (2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
- (3) Tested in accordance with JEDEC Standard 22, Test Method C101.

# SN65HVD50-SN65HVD59

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## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
$V_{I(K)}$	Input clamp voltage	$I_I = -18$ mA	-1.5			V	
$ V_{OD(SS)} $	Steady-state differential output voltage	$I_O = 0$	4		$V_{CC}$		
		$R_L = 54$ $\Omega$ , See <a href="#">Figure 1</a> (RS-485)	1.7	2.6			
		$R_L = 100$ $\Omega$ , See <a href="#">Figure 1</a> (RS-422)	2.4	3.2			
		$V_{test} = -7$ V to 12 V, See <a href="#">Figure 2</a>	1.6				
$\Delta V_{OD(SS)} $	Change in magnitude of steady-state differential output voltage between states	$R_L = 54$ $\Omega$ , See <a href="#">Figure 1</a> and <a href="#">Figure 2</a>	-0.2		0.2		
$V_{OD(RING)}$	Differential Output Voltage overshoot and undershoot	$R_L = 54$ $\Omega$ , $C_L = 50$ pF, See <a href="#">Figure 5</a> See <a href="#">Figure 3</a> for definition			10% <sup>(2)</sup>		
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	HVD50, HVD53, HVD56, HVD58		0.5			
		HVD51, HVD54, HVD57, HVD59	See <a href="#">Figure 4</a>	0.4			
		HVD52, HVD55		0.4			
$V_{OC(SS)}$	Steady-state common-mode output voltage	See <a href="#">Figure 4</a>	2.2		3.3		
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		-0.1		0.1		
$I_{Z(Z)}$ or $I_{Y(Z)}$	High-impedance state output current	HVD50, HVD51, HVD52, HVD56, HVD57	$V_{CC} = 0$ V, $V_Z$ or $V_Y = 12$ V, Other input at 0 V		90	$\mu$ A	
			$V_{CC} = 0$ V, $V_Z$ or $V_Y = -7$ V, Other input at 0 V	-10			
		HVD53, HVD54, HVD55, HVD58, HVD59	$V_{CC} = 5$ V or 0 V, DE = 0 V $V_Z$ or $V_Y = 12$ V	Other input at 0 V	90		
			$V_{CC} = 5$ V or 0 V, DE = 0 V $V_Z$ or $V_Y = -7$ V		-10		
$I_{Z(S)}$ or $I_{Y(S)}$	Short-circuit output current <sup>(3)</sup>	$V_Z$ or $V_Y = -7$ V	Other input at 0 V	-250	250	mA	
		$V_Z$ or $V_Y = 12$ V		-250	250		
$I_I$	Input current	D, DE	0		100	$\mu$ A	
$C_{(OD)}$	Differential output capacitance	$V_{OD} = 0.4 \sin(4E6\pi t) + 0.5$ V, DE at 0 V		16		pF	

(1) All typical values are at 25°C and with a 5-V supply.

(2) 10% of the peak-to-peak differential output voltage swing, per TIA/EIA-485

(3) Under some conditions of short-circuit to negative voltages, output currents exceeding the ANSI TIA/EIA-485-A maximum current of 250 mA may occur. Continuous exposure may affect device reliability.

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	HVD50, HVD53, HVD56, HVD58	4	8	12	ns
		HVD51, HVD54, HVD57, HVD59	20	29	46	
		HVD52, HVD55	90	143	230	
$t_{PHL}$	Propagation delay time, high-to-low-level output	HVD50, HVD53, HVD56, HVD58	4	8	12	ns
		HVD51, HVD54, HVD57, HVD59	20	30	46	
		HVD52, HVD55	90	143	230	
$t_r$	Differential output signal rise time	HVD50, HVD53, HVD56, HVD58	3	6	12	ns
		HVD51, HVD54, HVD57, HVD59	20	34	60	
		HVD52, HVD55	120	197	300	
$t_f$	Differential output signal fall time	HVD50, HVD53, HVD56, HVD58	3	6	11	ns
		HVD51, HVD54, HVD57, HVD59	20	33	60	
		HVD52, HVD55	120	192	300	
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )	HVD50, HVD53, HVD56, HVD58		1.4		ns
		HVD51, HVD54, HVD57, HVD59		1.6		
		HVD52, HVD55		7.4		
$t_{sk(pp)}^{(2)}$	Part-to-part skew	HVD50, HVD53, HVD56, HVD58		1		ns
		HVD51, HVD54, HVD57, HVD59		4		
		HVD52, HVD55		22		
$t_{PZH1}$	Propagation delay time, high-impedance-to-high-level output	HVD53, HVD58			30	ns
		HVD54, HVD59			180	
		HVD55			380	
$t_{PHZ}$	Propagation delay time, high-level-to-high-impedance output	HVD53, HVD58			16	ns
		HVD54, HVD59			40	
		HVD55			110	
$t_{PZL1}$	Propagation delay time, high-impedance-to-low-level output	HVD53, HVD58			23	ns
		HVD54, HVD59			200	
		HVD55			420	
$t_{PLZ}$	Propagation delay time, low-level-to-high-impedance output	HVD53, HVD58			19	ns
		HVD54, HVD59			70	
		HVD55			160	
$t_{PZH2}$	Propagation delay time, standby-to-high-level output	$R_L = 110 \Omega$ , $\overline{RE}$ at 3 V, See Figure 6 $D = 3 V$ and $S1 = Y$ , $D = 0 V$ and $S1 = Z$			3300	ns
$t_{PZL2}$	Propagation delay time, standby-to-low-level output	$R_L = 110 \Omega$ , $\overline{RE}$ at 3 V, See Figure 7 $D = 3 V$ and $S1 = Z$ , $D = 0 V$ and $S1 = Y$			3300	ns

(1) All typical values are at 25°C and with a 5-V supply.

 (2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

# SN65HVD50-SN65HVD59

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## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT			
$V_{IT+}$	Positive-going differential input threshold voltage	$I_O = -8$ mA			-0.02	V			
$V_{IT-}$	Negative-going differential input threshold voltage	$I_O = 8$ mA	-0.2						
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			50		mV			
$V_{IK}$	Enable-input clamp voltage	$I_I = -18$ mA	-1.5			V			
$V_O$	Output voltage	$V_{ID} = 200$ mV, $I_O = -8$ mA, See <a href="#">Figure 8</a>	4			V			
		$V_{ID} = -200$ mV, $I_O = 8$ mA, See <a href="#">Figure 8</a>			0.3				
$I_{O(Z)}$	High-impedance-state output current	$V_O = 0$ or $V_{CC}$ RE at $V_{CC}$	-1		1	$\mu$ A			
$I_A$ or $I_B$	Bus input current	HVD50, HVD53, HVD56, HVD58	Other input at 0 V	$V_A$ or $V_B = 12$ V	0.19	0.3	mA		
				$V_A$ or $V_B = 12$ V, $V_{CC} = 0$ V	0.24	0.4			
				$V_A$ or $V_B = -7$ V	-0.35	-0.19			
				$V_A$ or $V_B = -7$ V, $V_{CC} = 0$ V	-0.25	-0.14			
		HVD51, HVD52, HVD54, HVD55, HVD57, HVD59	Other input at 0 V	$V_A$ or $V_B = 12$ V	0.05	0.1	mA		
				$V_A$ or $V_B = 12$ V, $V_{CC} = 0$ V	0.06	0.1			
				$V_A$ or $V_B = -7$ V	-0.1	-0.05			
				$V_A$ or $V_B = -7$ V, $V_{CC} = 0$ V	-0.1	-0.03			
$I_{IH}$	Input current, $\overline{RE}$	$V_{IH} = 2$ V	-60			$\mu$ A			
		$V_{IL} = 0.8$ V	-60			$\mu$ A			
$C_{ID}$	Differential input capacitance	$V_{ID} = 0.4 \sin(4E6\pi t) + 0.5$ V, DE at 0 V		16		pF			
<b>Supply Current</b>									
$I_{CC}$	Supply current	HVD50, HVD51, HVD52, HVD56, HVD57, HVD53, HVD54, HVD55, HVD58, HVD59	D at 0 V or $V_{CC}$ and No Load		2.7	mA			
					8				
					9.5				
					2.3				
					2.9				
					4.5				
		HVD53, HVD54, HVD55, HVD58, HVD59	$\overline{RE}$ at $V_{CC}$ , D at $V_{CC}$ , DE at 0 V, No load (Receiver disabled and driver disabled)		0.08	1	$\mu$ A		
				HVD53, HVD54, HVD55, HVD58, HVD59	$\overline{RE}$ at 0 V, D at 0 V or $V_{CC}$ , DE at $V_{CC}$ , No load (Receiver enabled and driver enabled)		2.7	mA	
							8		
							4.3		
							9.7		
				HVD53, HVD54, HVD55, HVD58, HVD59	$\overline{RE}$ at $V_{CC}$ , D at 0 V or $V_{CC}$ , DE at $V_{CC}$ , No load (Receiver disabled and driver enabled)		2.3		mA
							7.7		
							3.2		
	8.5								

(1) All typical values are at 25°C and with a 5-V supply.

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	HVD50, HVD53, HVD56, HVD58		24	40	ns
		HVD51, HVD52, HVD54, HVD55, HVD57, HVD59		43	55	
$t_{PHL}$	Propagation delay time, high-to-low-level output	HVD50, HVD53, HVD56, HVD58		26	35	
		HVD51, HVD52, HVD54, HVD55, HVD57, HVD59		47	60	
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )	HVD50, HVD53, HVD56, HVD57, HVD58, HVD59	$V_{ID} = -1.5\text{ V to }1.5\text{ V},$ $C_L = 15\text{ pF},$ See <a href="#">Figure 9</a>		5	
		HVD51, HVD54, HVD52, HVD55			7	
$t_{sk(pp)}^{(2)}$	Part-to-part skew	HVD50, HVD53, HVD56, HVD58		5		
		HVD51, HVD54, HVD57, HVD59		6		
		HVD52, HVD55		6		
$t_r$	Output signal rise time		2.3	4		
$t_f$	Output signal fall time		2.4	4		
$t_{PHZ}$	Output disable time from high level	DE at 3 V, $C_L = 15\text{ pF}$ See <a href="#">Figure 10</a>			17	
$t_{PZH1}$	Output enable time to high level				10	
$t_{PZH2}$	Propagation delay time, standby-to-high-level output	DE at 0 V, $C_L = 15\text{ pF}$ See <a href="#">Figure 10</a>			3300	
$t_{PLZ}$	Output disable time from low level	DE at 3 V, $C_L = 15\text{ pF}$ See <a href="#">Figure 11</a>			13	
$t_{PZL1}$	Output enable time to low level				10	
$t_{PZL2}$	Propagation delay time, standby-to-low-level output	DE at 0 V, $C_L = 15\text{ pF}$ See <a href="#">Figure 11</a>			3300	

(1) All typical values are at 25°C and with a 5-V supply

 (2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

# SN65HVD50-SN65HVD59

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## RECEIVER EQUALIZATION CHARACTERISTICS

 over recommended operating conditions unless otherwise noted<sup>(1)</sup>

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>(2)</sup>	MAX	UNIT
$t_{j(pp)}$	Peak-to-peak eye-pattern jitter	Pseudo-random NRZ code with a bit pattern length o 216-1, Belden 3105A cable	25 Mbps	0 m	HVD56, HVD58		PREVIEW	ns
				100 m	HVD53		PREVIEW	
					HVD56, HVD58		PREVIEW	
				150 m	HVD53		PREVIEW	
					HVD56, HVD58		PREVIEW	
				200 m	HVD53		PREVIEW	
			HVD56, HVD58			PREVIEW		
			10 Mbps	200 m	HVD53		PREVIEW	
					HVD56, HVD58		PREVIEW	
				250 m	HVD53		PREVIEW	
					HVD56, HVD58		PREVIEW	
				300 m	HVD53		PREVIEW	
					HVD56, HVD58		PREVIEW	
			5 Mbps	500 m	HVD54		PREVIEW	
					HVD57, HVD59		PREVIEW	
			3 Mbps	500 m	HVD53		PREVIEW	
					HVD54		PREVIEW	
					HVD56, HVD58		PREVIEW	
					HVD57, HVD59		PREVIEW	
			1 Mbps	1000 m	HVD54		PREVIEW	
HVD57, HVD59		PREVIEW						

(1) The HVD53 and HVD54 do not have receiver equalization but are specified for comparison.

 (2) All typical values are at  $V_{CC} = 5\text{ V}$ , and temperature = 25°C.

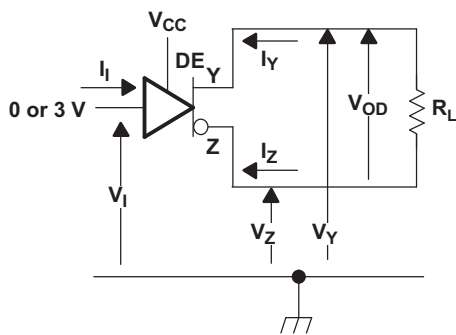
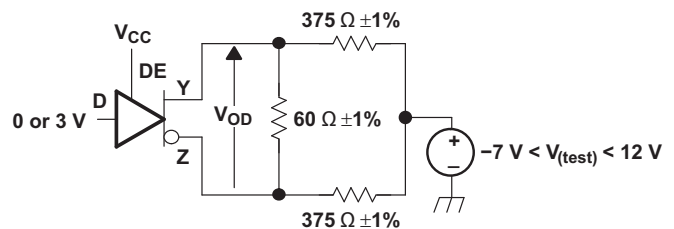


**THERMAL CHARACTERISTICS**

 over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

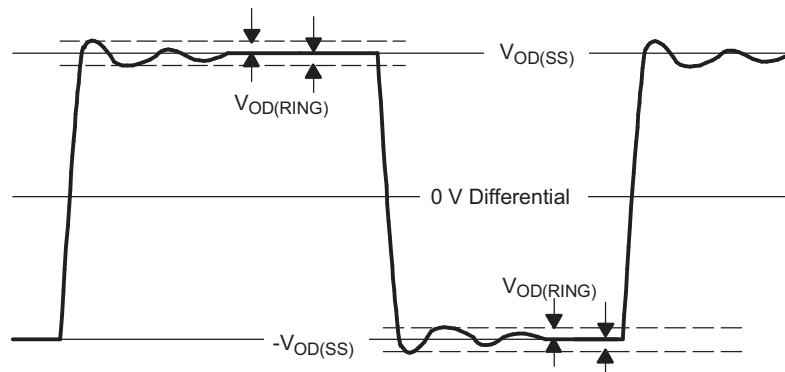
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	Low-K board <sup>(3)</sup> , No airflow	HVD50, HVD51, HVD52, HVD56, HVD57		230.8	°C/W	
			HVD53, HVD54, HVD55, HVD58, HVD59		162.6		
	Junction-to-ambient thermal resistance <sup>(2)</sup>	High-K board <sup>(4)</sup> , No airflow	HVD50, HVD51, HVD52, HVD56, HVD57		135.1		
			HVD53, HVD54, HVD55, HVD58, HVD59		92.1		
$\theta_{JB}$	Junction-to-board thermal resistance	High-K board	HVD50, HVD51, HVD52, HVD56, HVD57		44.4		
			HVD53, HVD54, HVD55, HVD58, HVD59		61.1		
$\theta_{JC}$	Junction-to-case thermal resistance	No board	HVD50, HVD51, HVD52, HVD56, HVD57		43.5		
			HVD53, HVD54, HVD55, HVD58, HVD59		58.6		
$P_D$	Device power dissipation	$R_L = 60\Omega$ , $C_L = 50$ pF, Input to D a 50% duty cycle square wave at indicated signaling rate	HVD50, HVD56 (25Mbps)		420	mW	
			HVD51, HVD57 (10Mbps)		404		
			HVD52 (1Mbps)		383		
		$R_L = 60\Omega$ , $C_L = 50$ pF, DE at $V_{CC}$ RE at 0 V, Input to D a 50% duty cycle square wave at indicated signaling rate	HVD53, HVD58 (25Mbps)		420		
			HVD54, HVD59 (10Mbps)		404		
			HVD55 (1Mbps)		383		
$T_A$	Ambient air temperature	Low-K board, No airflow	HVD50, HVD56		-40	°C	
			HVD51, HVD52, HVD57		-40		84
			HVD53, HVD54, HVD55, HVD58, HVD59		-40		85
		High-K board, No airflow	HVD50, HVD51, HVD52, HVD56, HVD57		-40		85
			HVD53, HVD54, HVD55, HVD58, HVD59		-40		85
$T_{JSD}$	Thermal shutdown junction temperature			165			

- (1) See *Application Information* section for an explanation of these parameters.
- (2) The intent of  $\theta_{JA}$  specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
- (3) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
- (4) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

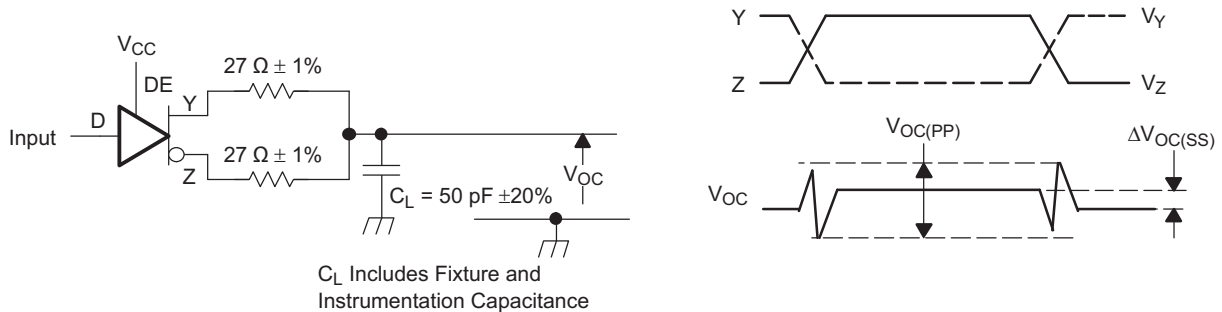
**PARAMETER MEASUREMENT INFORMATION**

**Figure 1. Driver  $V_{OD}$  Test Circuit: Voltage and Current Definitions**

**Figure 2. Driver  $V_{OD}$  With Common-Mode Loading Test Circuit**

## PARAMETER MEASUREMENT INFORMATION (continued)

VOD(RING) is measured at four points on the output waveform, corresponding to overshoot and undershoot from the VOD(H) and VOD(L) steady state values.

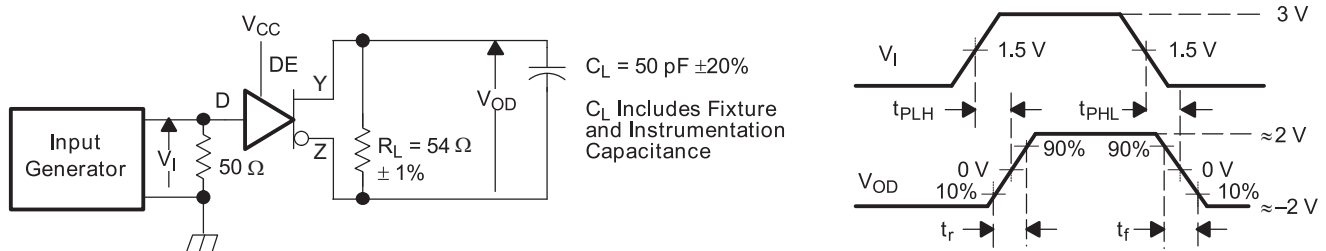


**Figure 3. V<sub>OD(RING)</sub> Waveform and Definitions**



Input: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6\text{ns}$ ,  $t_f < 6\text{ns}$ ,  $Z_O = 50\ \Omega$

**Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**



Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6\ \text{ns}$ ,  $t_f < 6\ \text{ns}$ ,  $Z_O = 50\ \Omega$

**Figure 5. Driver Switching Test Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION (continued)

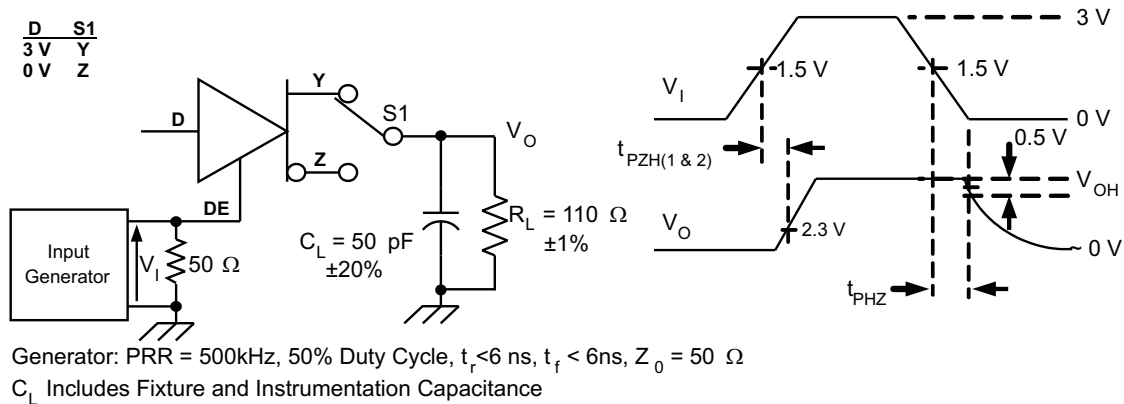


Figure 6. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

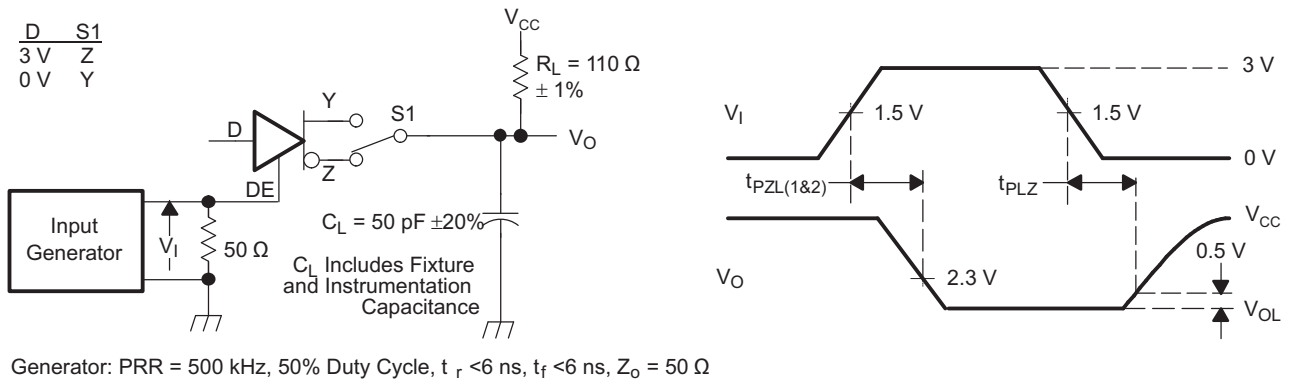


Figure 7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

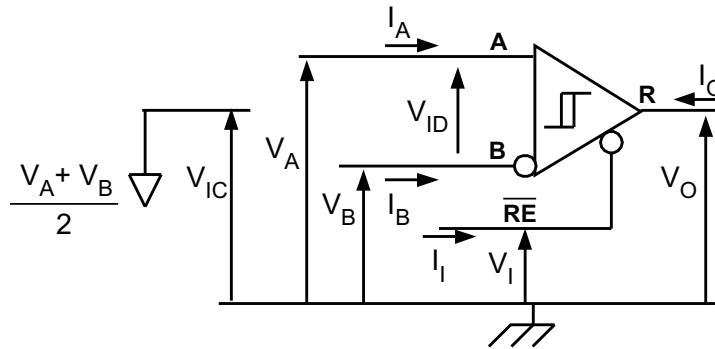
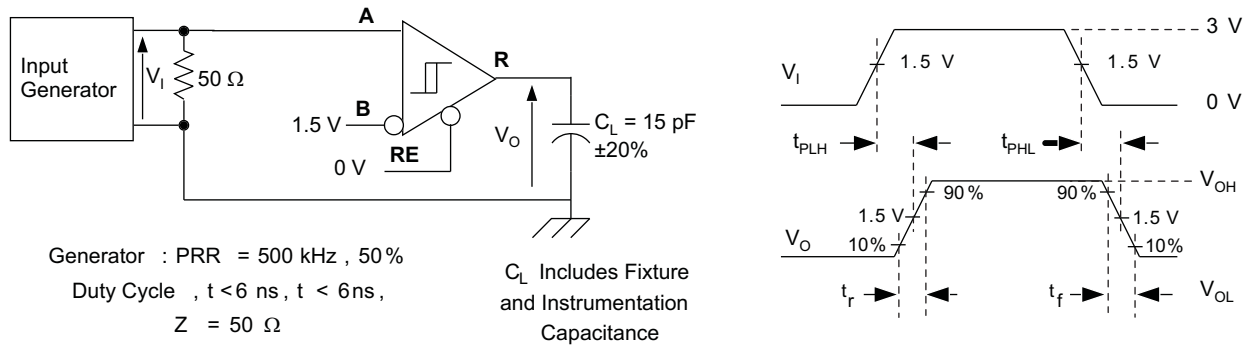
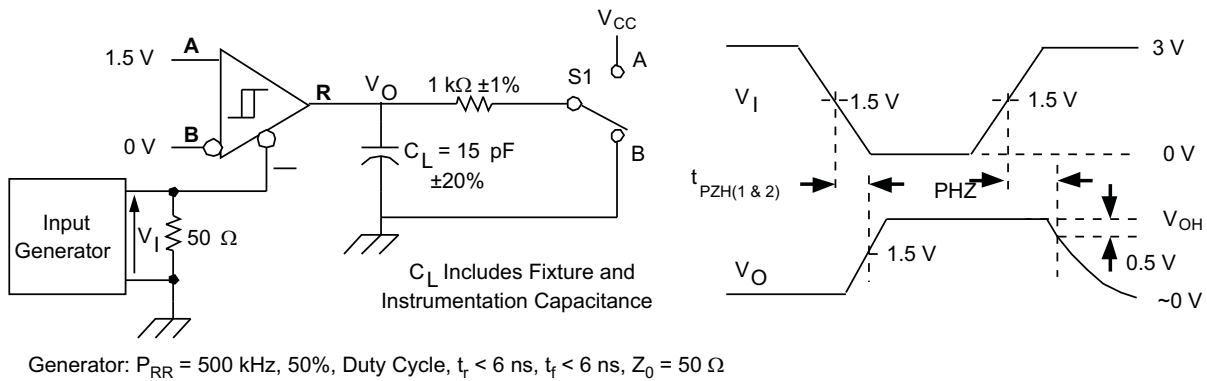


Figure 8. Receiver Voltage and Current Definitions

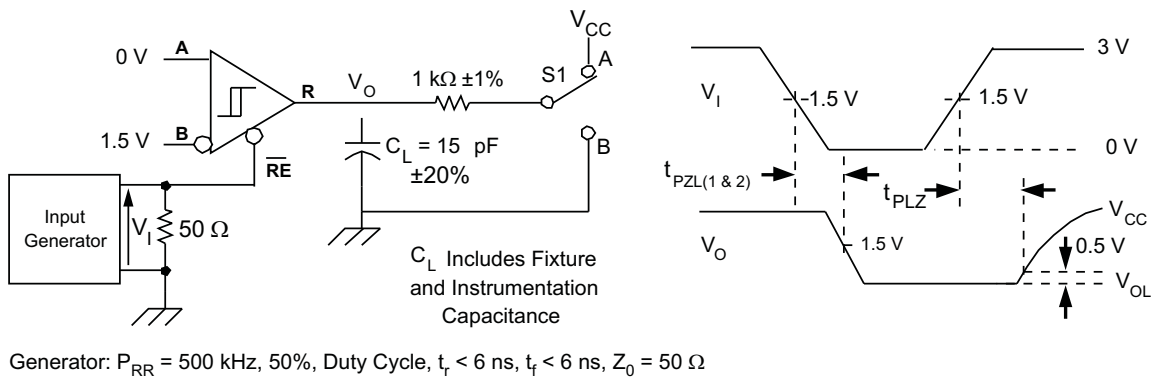
**PARAMETER MEASUREMENT INFORMATION (continued)**



**Figure 9. Receiver Switching Test Circuit and Voltage Waveforms**



**Figure 10. Receiver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms**



**Figure 11. Receiver Low-Level Enable and Disable Time Test Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION (continued)

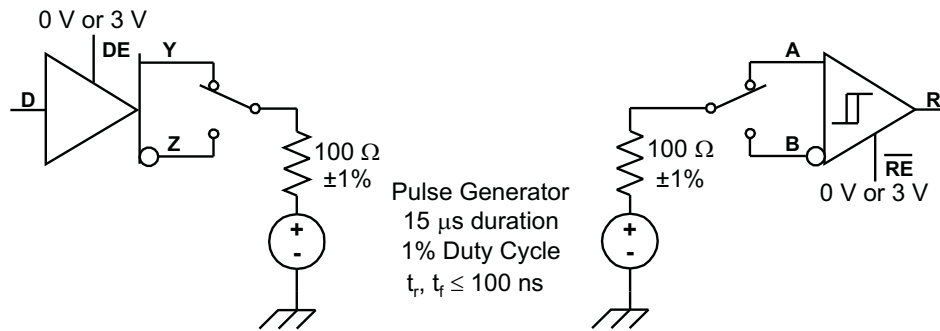


Figure 12. Test Circuit, Transient Overvoltage Test

DEVICE INFORMATION

LOW-POWER STANDBY MODE

When both the driver and receiver are disabled (DE low and  $\overline{RE}$  high) the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

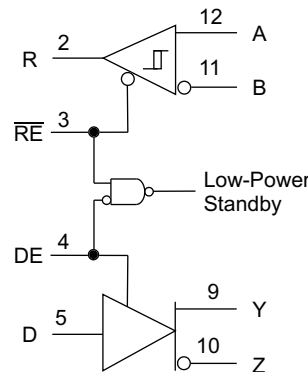


Figure 13. Low-Power Standby Logic Diagram

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the D input after the enable times given by  $t_{PZH2}$  and  $t_{PZL2}$  in the driver switching characteristics. If the D input is open when the driver is enabled, the driver outputs default to A high and B low, in accordance with the driver failsafe feature.

If only the receiver is re-enabled ( $\overline{RE}$  transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by  $t_{PZH2}$  and  $t_{PZL2}$  in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

**FUNCTION TABLES**
**SN65HVD53, SN65HVD54, SN65HVD55, SN65HVD58,  
SN65HVD59 DRIVER**

INPUTS		OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L or open	Z	Z
Open	H	L	H

**SN65HVD53, SN65HVD54, SN65HVD55, SN65HVD58,  
SN65HVD59 RECEIVER**

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \leq -0.2\text{ V}$	L	L
$-0.2\text{ V} < V_{ID} < -0.02\text{ V}$	L	?
$-0.02\text{ V} \leq V_{ID}$	L	H
X	H or open	Z
Open Circuit	L	H
Idle circuit	L	H
Short Circuit, $V_{(A)} = V_{(B)}$	L	H

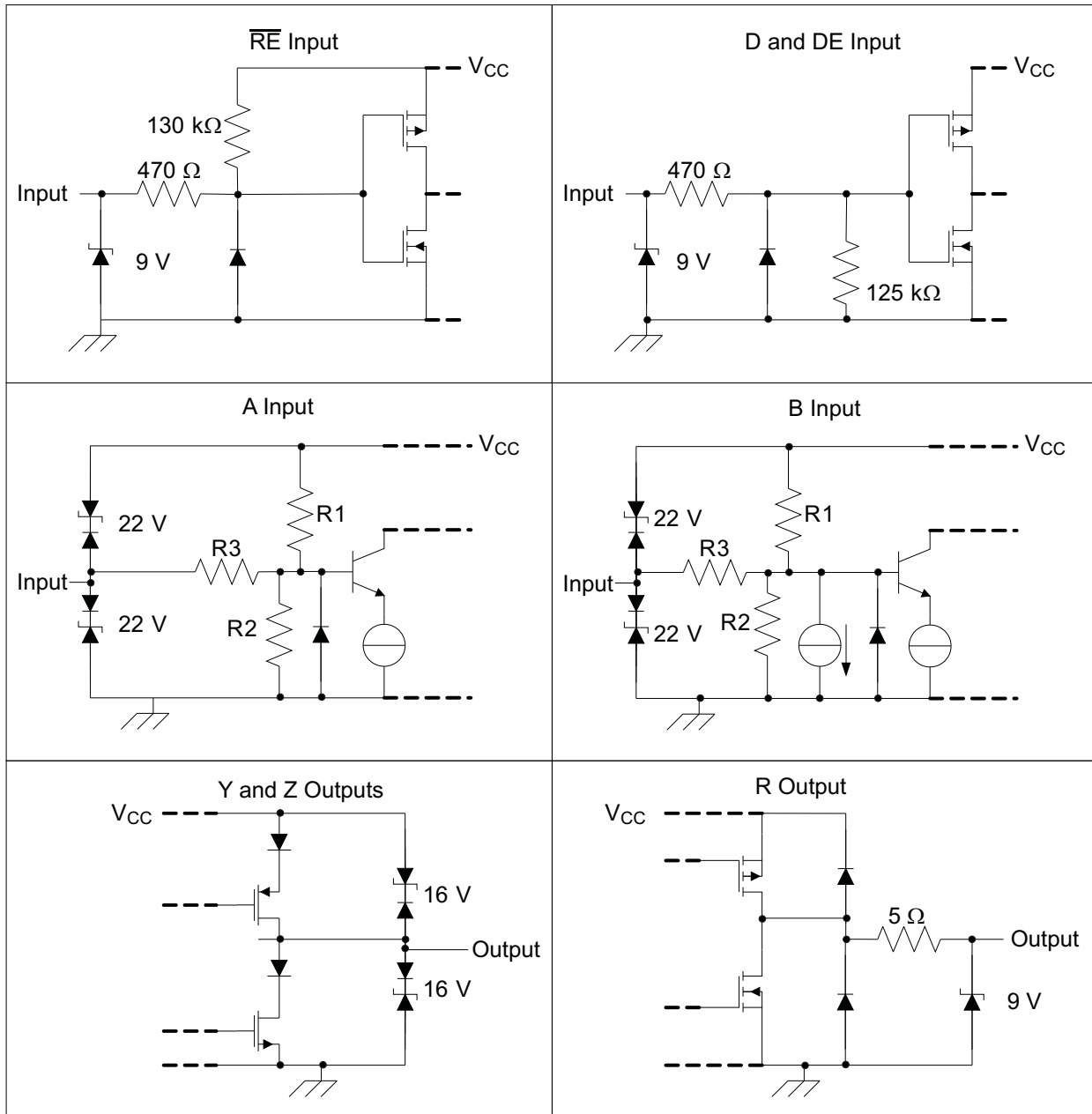
**SN65HVD50, SN65HVD51, SN65HVD52, SN65HVD56,  
SN65HVD57 DRIVER**

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H
Open	L	H

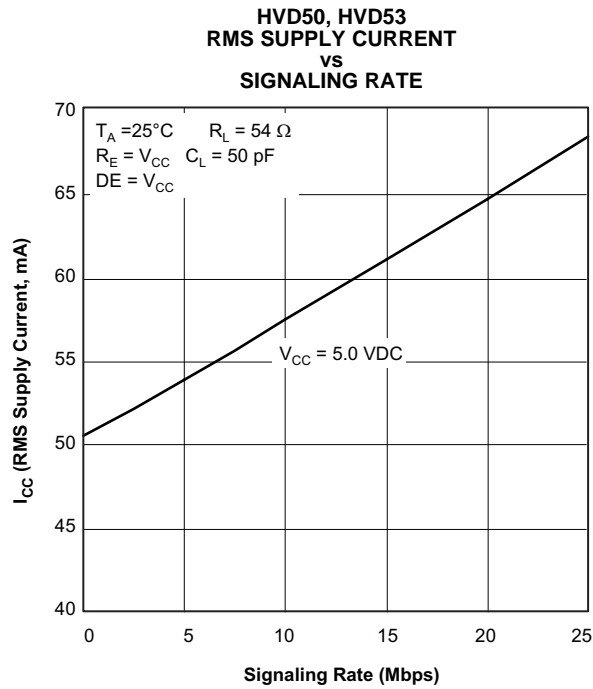
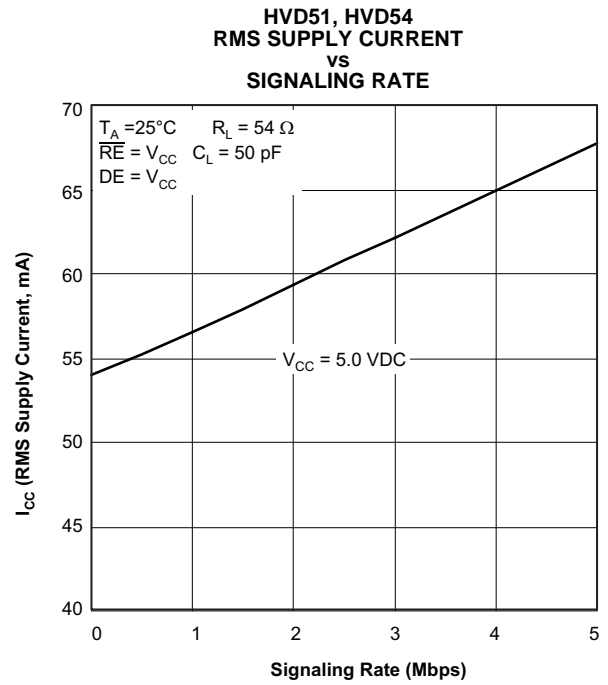
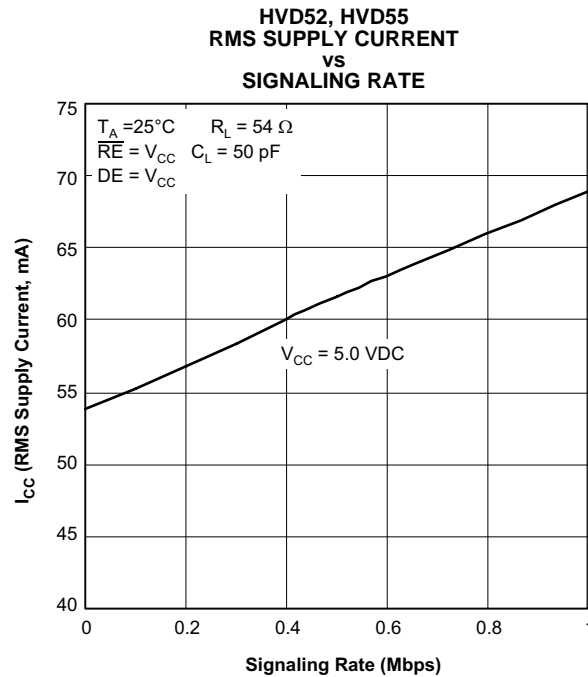
**SN65HVD50, SN65HVD51, SN65HVD52, SN65HVD56,  
SN65HVD57 RECEIVER**

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	OUTPUT R
$V_{ID} \leq -0.2\text{ V}$	L
$-0.2\text{ V} < V_{ID} < -0.02\text{ V}$	?
$-0.02\text{ V} \leq V_{ID}$	H
Open Circuit	H
Idle circuit	H
Short Circuit, $V_{(A)} = V_{(B)}$	H

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



	R1/R2	R3
SN65HVD50, SN65HVD53, SN65HVD56, SN65HVD58	9 kΩ	45 kΩ
SN65HVD51, SN65HVD52, SN65HVD54, SN65HVD55, SN65HVD57, SN65HVD58, SN65HVD59	36 kΩ	180 kΩ

**TYPICAL CHARACTERISTICS**

**Figure 14.**

**Figure 15.**

**Figure 16.**



TYPICAL CHARACTERISTICS (continued)

HVD50, HVD53  
BUS INPUT CURRENT  
VS  
INPUT VOLTAGE

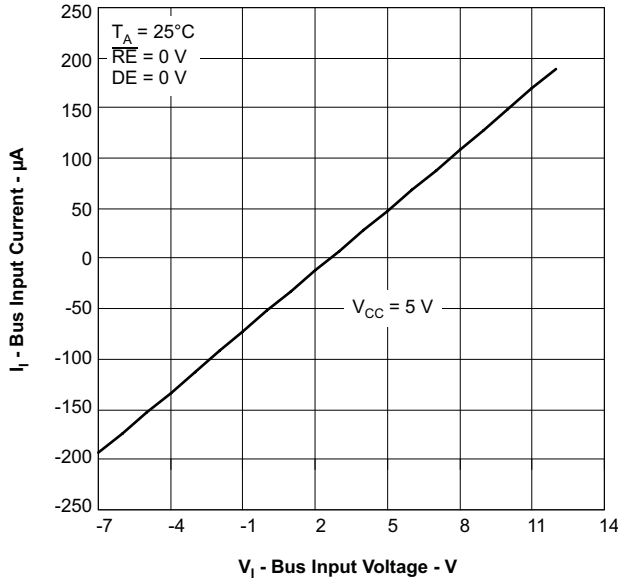


Figure 17.

HVD51, HVD52, HVD54, HVD55  
BUS INPUT CURRENT  
VS  
INPUT VOLTAGE

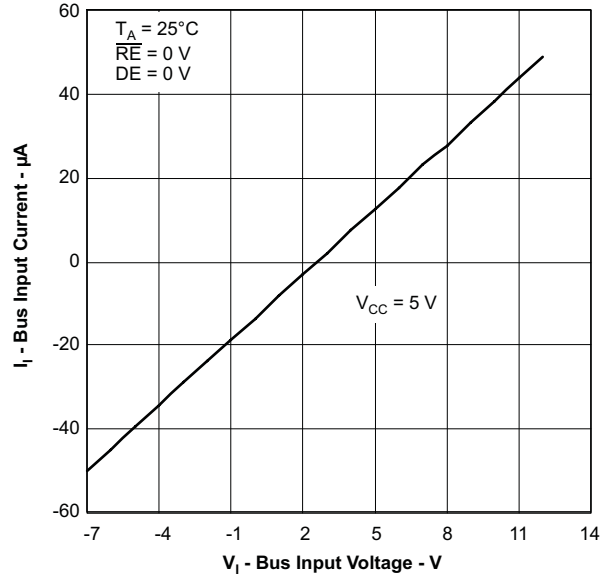


Figure 18.

DRIVER LOW-LEVEL OUTPUT CURRENT  
VS  
LOW-LEVEL OUTPUT VOLTAGE

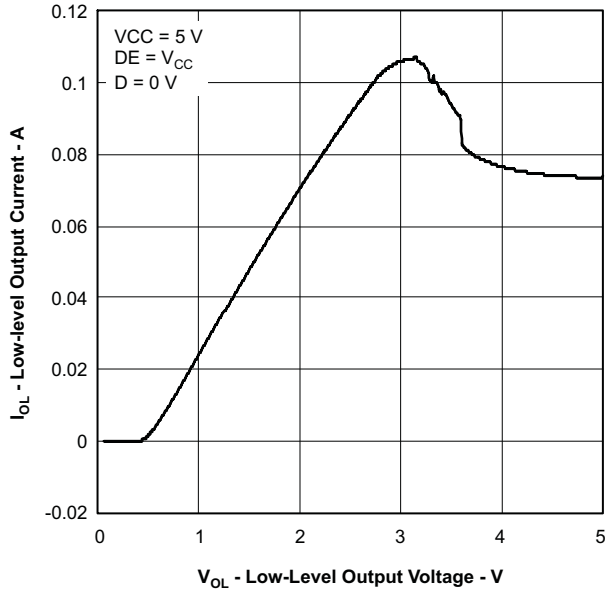


Figure 19.

DRIVER HIGH-LEVEL OUTPUT CURRENT  
VS  
HIGH-LEVEL OUTPUT VOLTAGE

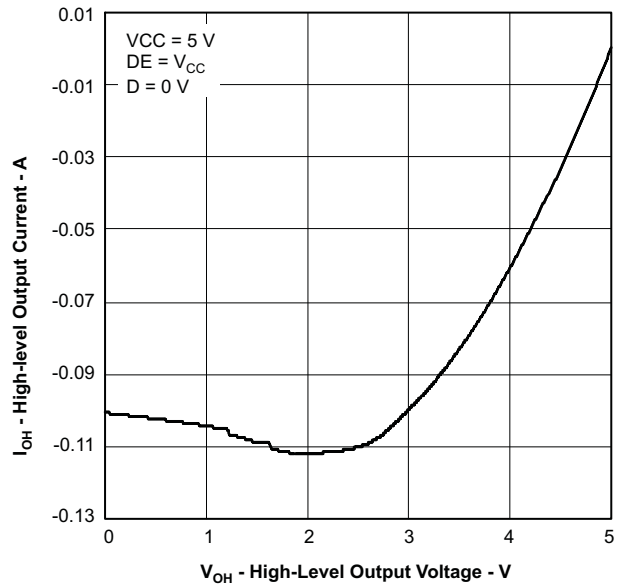


Figure 20.

TYPICAL CHARACTERISTICS (continued)

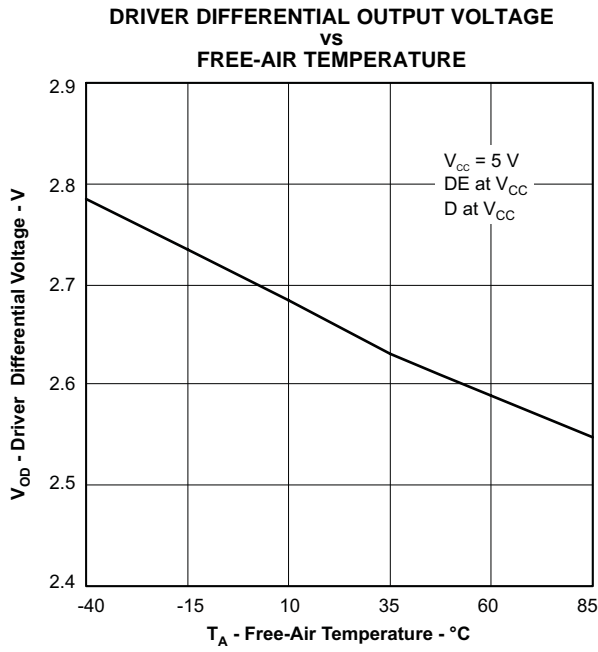


Figure 21.

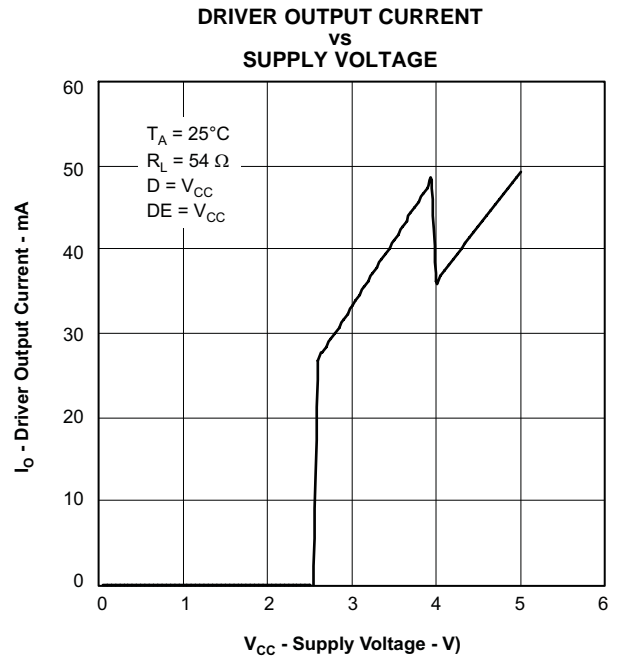


Figure 22.

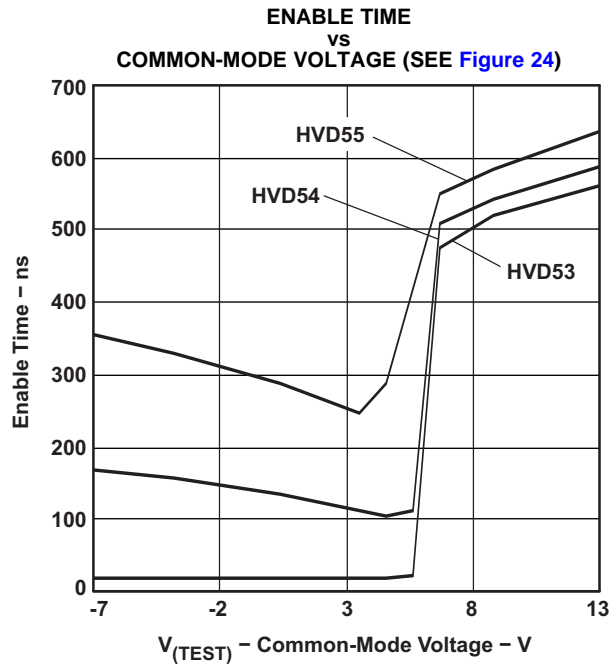


Figure 23.

TYPICAL CHARACTERISTICS (continued)

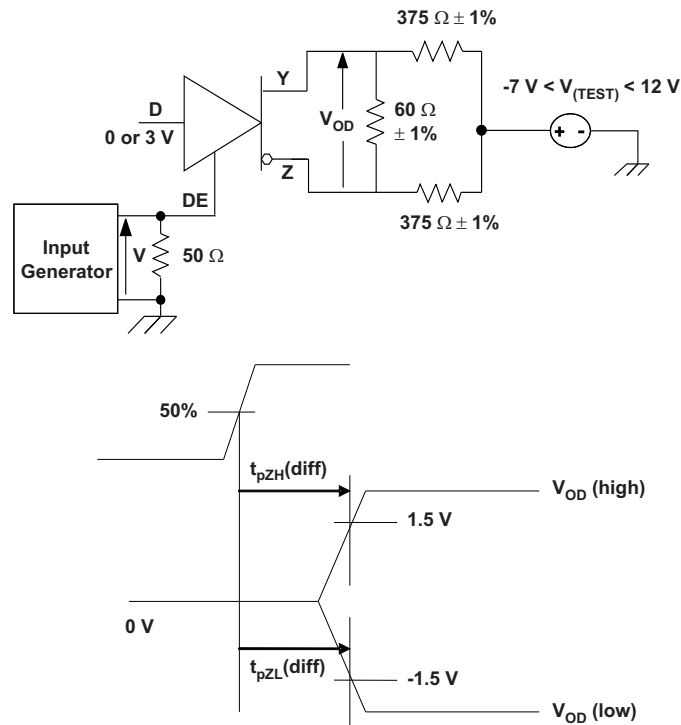


Figure 24. Driver Enable Time From DE to  $V_{OD}$

The time  $t_{pZL(x)}$  is the measure from DE to  $V_{OD}(x)$ .  $V_{OD}$  is valid when it is greater than 1.5 V.

## APPLICATION INFORMATION

### THERMAL CHARACTERISTICS OF IC PACKAGES

$\theta_{JA}$  (**Junction-to-Ambient Thermal Resistance**) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

$\theta_{JA}$  is not a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

$\theta_{JA}$  can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures.  $\theta_{JA}$  is often misused when it is used to calculate junction temperatures for other installations.

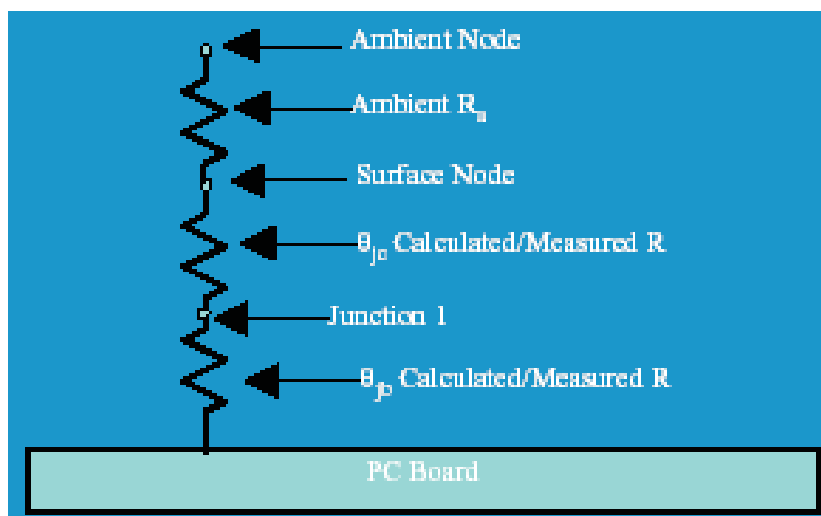
TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-k board gives *best case* in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in  $\theta_{JA}$  can be measured between these two test cards

$\theta_{JC}$  (**Junction-to-Case Thermal Resistance**) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

$\theta_{JC}$  is a useful thermal characteristic when a heatsink applied to package. It is *not* a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with  $\theta_{JB}$  in 1-dimensional thermal simulation of a package system.

$\theta_{JB}$  (**Junction-to-Board Thermal Resistance**) is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure.  $\theta_{JB}$  is only defined for the high-k test card.

$\theta_{JB}$  provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system, see [Figure 25](#).



**Figure 25. Thermal Resistance**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65HVD50D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD50DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD50DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD50DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD51D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD51DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD51DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD51DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD52D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD52DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD52DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD52DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD53D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD53DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD53DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD53DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD54D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD54DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD54DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD54DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD55D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD55DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD55DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD55DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

---

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD50DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD51DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD52DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD53DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD54DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65HVD55DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



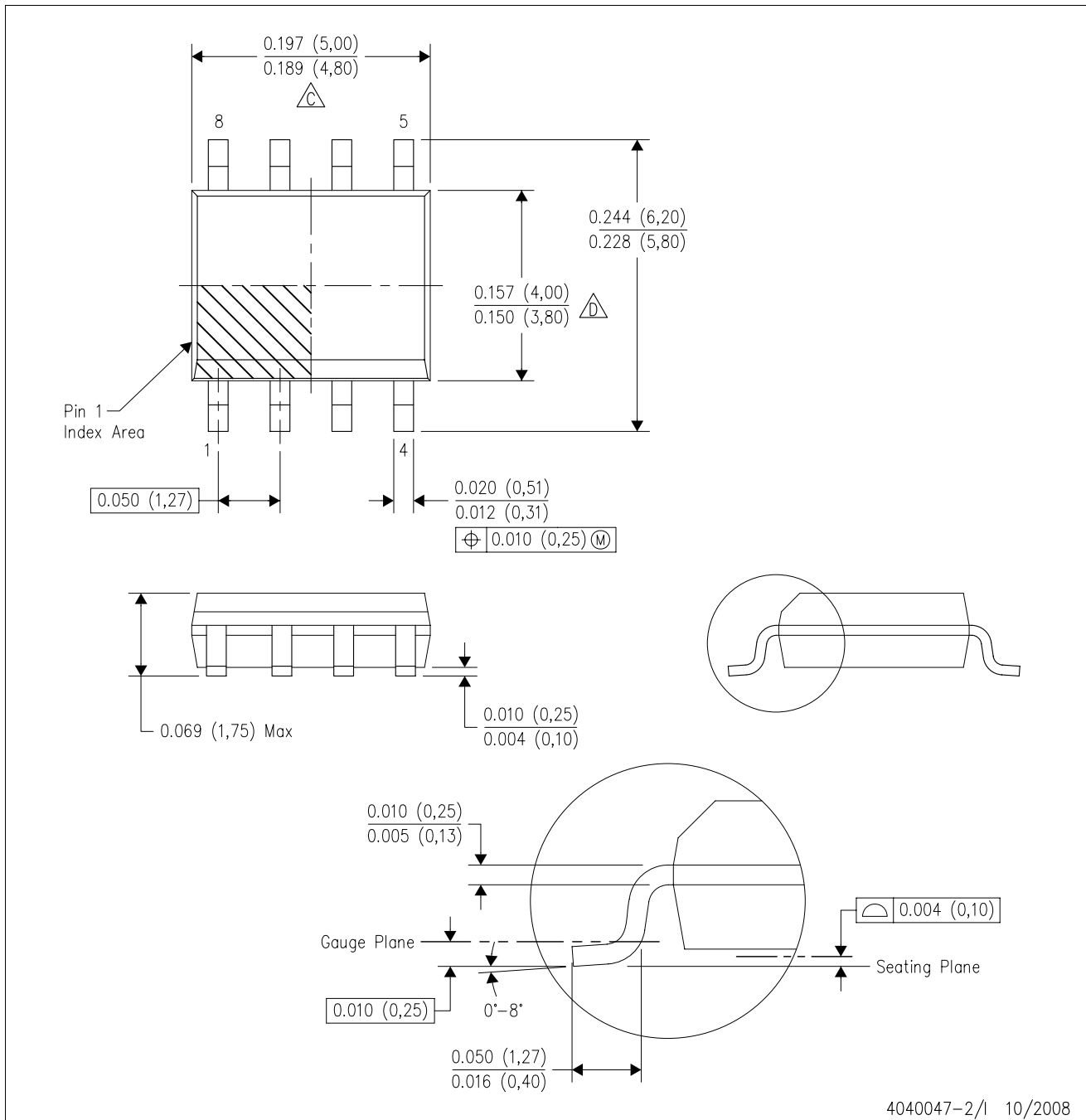
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD50DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD51DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD52DR	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD53DR	SOIC	D	14	2500	346.0	346.0	33.0
SN65HVD54DR	SOIC	D	14	2500	346.0	346.0	33.0
SN65HVD55DR	SOIC	D	14	2500	346.0	346.0	33.0



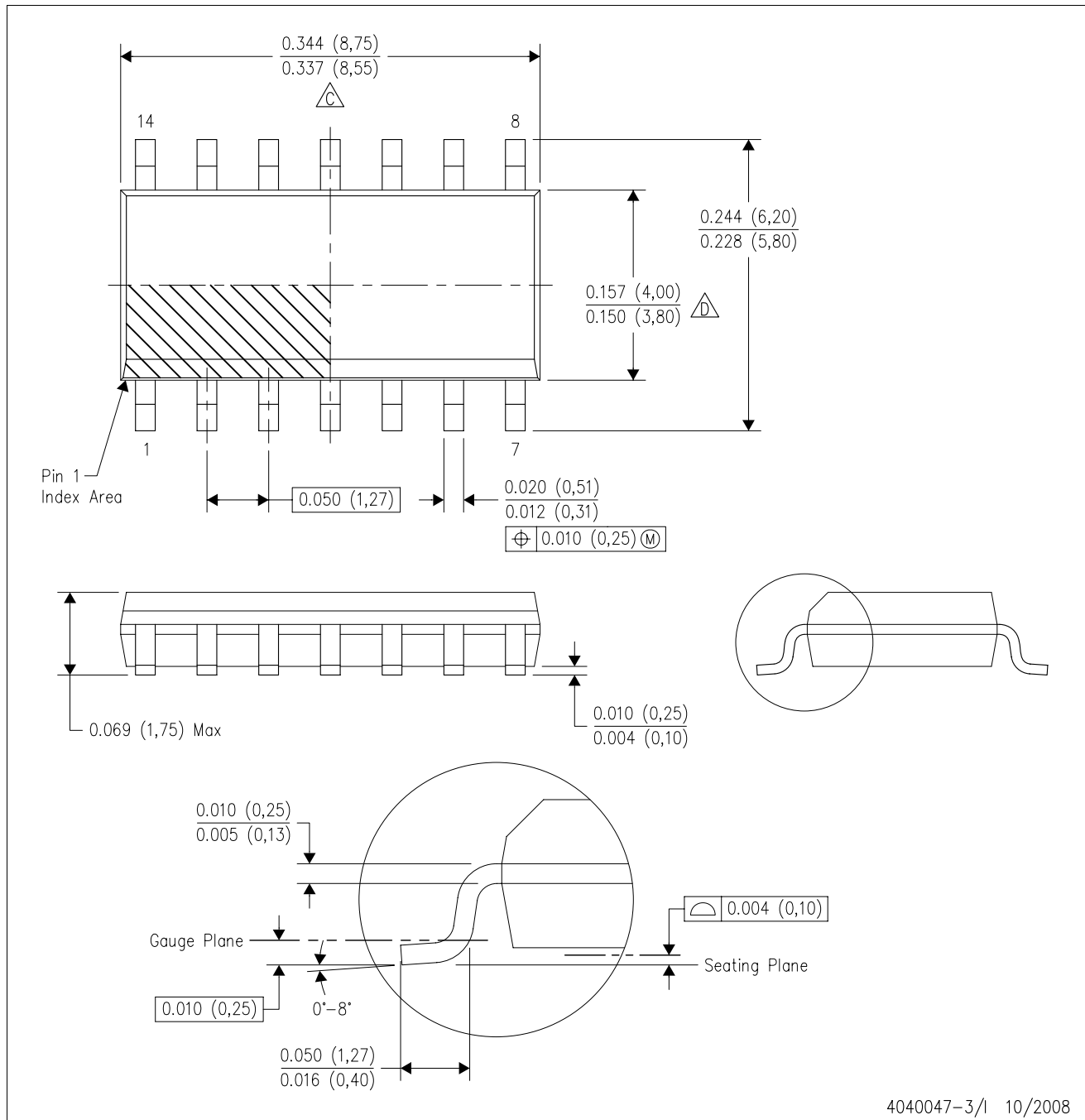
D (R-PDSO-G8)



PLASTIC SMALL-OUTLINE PACKAGE



D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  -  Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.

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