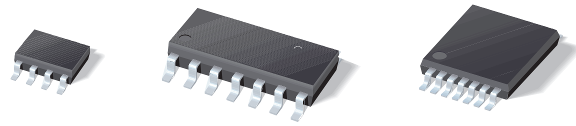


SLOS382 − SEPTEMBER 2001

LOW-NOISE, HIGH-SPEED, 450 mA CURRENT FEEDBACK AMPLIFIERS

FEATURES

- **Low Noise**
  - **2.9 pA/√Hz Noninverting Current Noise**
  - **10.8 pA/√Hz Inverting Current Noise**
  - **2.2 nV/√Hz Voltage Noise**
- **High Output Current, 450 mA**
- **High Speed**
  - **128 MHz , −3 dB BW(R_L = 50 Ω, R_F = 470 Ω)**
  - **1550 V/µs Slew Rate (G = 2, R_L = 50 Ω)**
- **Wide Output Swing**
  - **26 V_{PP} Output Voltage, R_L = 50 Ω**
- **Low Distortion**
  - **-80 dBc (1 MHz, 2 V_{PP}, G = 2)**
- **Low Power Shutdown Mode (THS3125)**
  - **370-µA Shutdown Supply Current**
- **Standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD Package**

APPLICATIONS

- **Video Distribution**
- **Instrumentation**
- **Line Drivers**
- **Motor Drivers**
- **Piezo Drivers**

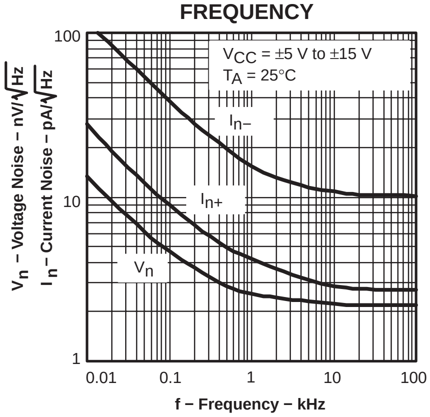
DESCRIPTION

The THS3122/5 are low-noise, high-speed current feedback amplifiers, with high output current drive. This makes them ideal for any application that requires low distortion over a wide frequency with heavy loads. The THS3122/5 can drive four serially terminated video lines while maintaining a differential gain error less than 0.03%.

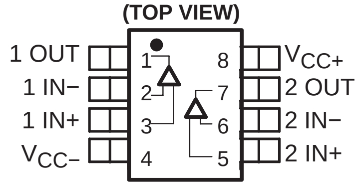
The high output drive capability of the THS3122/5 enables the devices to drive 50-Ω loads with low distortion over a wide range of output voltages:
−80 −dBc THD at 2 V_{PP}
−75 −dBc THD at 8 V_{PP}

The THS3122/5 can operate from ±5 V to ±15 V supply voltages while drawing as little as 7.2 mA of supply current per channel. They offer a low power shutdown mode, reducing the supply current to only 370 µA. The THS3122/5 are packaged in a standard SOIC, SOIC PowerPAD™, and TSSOP PowerPAD packages.

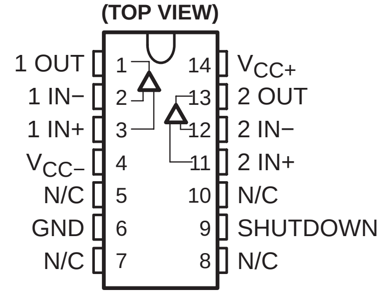
VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY



**THS3122
SOIC (D) AND
SOIC PowerPAD™ (DDA) PACKAGE
(TOP VIEW)**



**THS3125
SOIC (D) AND
TSSOP PowerPAD™ (PWP) PACKAGE
(TOP VIEW)**



AVAILABLE OPTIONS

T_A	PACKAGED DEVICE				EVALUATION MODULES
	SOIC-8 (D)	SOIC-8 PowerPAD (DDA)	SOIC-14 (D)	TSSOP-14 (PWP)	
0°C to 70°C	THS3122CD	THS3122CDDA	THS3125CD	THS3125CPWP	THS3122EVM THS3125EVM
−40°C to 85°C	THS3122ID	THS3122IDDA	THS3125ID	THS3125IPWP	

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} to V_{CC-}	33 V
Input voltage	± V_{CC}
Output current (see Note 1)	275 mA
Differential input voltage	± 4 V
Maximum junction temperature	150°C
Total power dissipation at (or below) 25°C free-air temperature	See Dissipation Ratings Table
Operating free-air temperature, T_A: Commercial	0°C to 70°C
Operating free-air temperature, T_A: Industrial	−40°C to 85°C
Storage temperature, T_{stg}: Commercial	−65°C to 125°C
Storage temperature, T_{stg}: Industrial	−65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS3122 and THS3125 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA}	T_A = 25°C POWER RATING
D-8	95°C/W‡	1.32 W
DDA	67°C/W	1.87 W
D-14	66.6°C/W‡	1.88 W
PWP	37.5°C/W	3.3 W

‡ This data was taken using the JEDEC proposed high-K test PCB. For the JEDEC low-K test PCB, the θ_{JA} is168°C/W for the D-8 package and 122.3°C/W for the D-14 package.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} to V_{CC-}	Dual supply	±5		±15	V
	Single supply	10		30	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	−40		85	
Shutdown pin input levels, relative to the GND pin	High level (device shutdown)	2			V
	Low level (device active)			0.8	

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±15 V, R_F= 750 Ω, R_L = 100 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (−3 dB)	R_L = 50 Ω	R_F = 50 Ω, G = 1	V_{CC} = ±5 V		138		MHz
				V_{CC} = ±15 V		160		
		R_L = 50 Ω	R_F =470 Ω, G = 2	V_{CC} = ±5 V		126		
				V_{CC} = ±15 V		128		
	Bandwidth (0.1 dB)		R_F = 470 Ω, G = 2	V_{CC} = ±5 V		20		
				V_{CC} = ±15 V		30		
	Full power bandwidth	G = −1	$V_{O(PP)}$ = 4 V	V_{CC} = ±5 V		47		MHz
			$V_{O(pp)}$ = 20 V	V_{CC} = ±15 V		64		
SR	Slew rate (see Note 2), G=8	G = 2, R_F = 680 Ω	V_O = 10 V_{PP}	V_{CC} = ±15 V		1550		V/µs
			V_O = 5 V_{PP}	V_{CC} = ±5 V		500		
				V_{CC} = ±15 V		1000		
t_s	Settling time to 0.1%	G = −1	V_O = 2 V_{PP}	V_{CC} = ±5 V		53		ns
			V_O = 5 V_{PP}	V_{CC} = ±15 V		64		

NOTE 2: Slew rate is defined from the 25% to the 75% output levels.

noise/distortion performance

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion		G = 2, R_F = 470 Ω, V_{CC} = ±15 V, f = 1 MHz	$V_{O(PP)}$ = 2 V		−80		dBc
				$V_{O(PP)}$ = 8 V		−75		
			G = 2, R_F = 470 Ω, V_{CC} = ±5 V, f = 1 MHz	$V_{O(PP)}$ = 2 V		−77		
				$V_{O(PP)}$ = 5 V		−76		
V_n	Input voltage noise		V_{CC} = ±5 V, ±15 V	f = 10 kHz		2.2		nV/√Hz
I_n	Input current noise	Noninverting Input	V_{CC} = ±5 V, ±15 V	f = 10 kHz		2.9		pA/√Hz
		Inverting Input				10.8		
	Crosstalk		G = 2, f = 1 MHz, V_O = 2 V_{PP}	V_{CC} = ±5 V		−67		dBc
				V_{CC} = ±15 V		−67		
	Differential gain error		G = 2, R_L = 150 Ω, 40 IRE modulation, ±100 IRE Ramp, NTSC and PAL	V_{CC} = ±5 V		0.01%		
				V_{CC} = ±15 V		0.01%		
	Differential phase error			V_{CC} = ±5 V		0.011°		
				V_{CC} = ±15 V		0.011°		

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±15 V, R_F = 750 Ω, R_L = 100 Ω (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, V_{CC} = ±5 V, V_{CC} = ±15 V	T_A = 25°C		4.4	6	mV
			T_A = full range			8	mV
	Channel offset voltage matching		T_A = 25°C		0.4	2	mV
			T_A = full range			3	mV
	Offset drift		T_A = full range		10		μV/°C
I_{IB}	IN− Input bias current	V_{IC} = 0 V, V_O = 0 V, V_{CC} = ±5 V, V_{CC} = ±15 V	T_A = 25°C		6	23	μA
			T_A = full range			30	μA
	IN+ Input bias current		T_A = 25°C		0.33	2	μA
			T_A = full range			3	μA
I_{IO}	Input offset current	V_{IC} = 0 V, V_O = 0 V, V_{CC} = ±5 V, V_{CC} = ±15 V	T_A = 25°C		5.4	22	μA
			T_A = full range			30	μA
Z_{OL}	Open loop transimpedance	V_{CC} = ±5 V, V_{CC} = ±15 V	R_L = 1 kΩ,		1		MΩ

input characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Input common-mode voltage range	V_{CC} = ±5 V	T_A = full range	±2.5	±2.7		V
		V_{CC} = ±15 V		±12.5	±12.7		V
CMRR	Common-mode rejection ratio	V_{CC} = ±5 V, V_I = −2.5 V to 2.5 V	T_A = 25°C	58	62		dB
			T_A = full range	56			dB
		V_{CC} = ±15 V, V_I = −12.5 V to 12.5 V	T_A = 25°C	63	67		dB
			T_A = full range	60			dB
R_I	Input resistance	IN+			1.5		MΩ
		IN−			15		Ω
C_i	Input capacitance				2		pF

output characteristics

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_O	Output voltage swing	G = 4, V_I = 1.06 V, V_{CC} = ±5 V	R_L = 1 kΩ,	T_A = 25°C		4.1		V
		G = 4, V_I = 1.025 V, V_{CC} = ±5 V	R_L = 50 Ω,	T_A = 25°C	3.8	4		V
				T_A = full range	3.7			V
		G = 4, V_I = 3.6 V, V_{CC} = ±15 V	R_L = 1 kΩ,	T_A = 25°C		14.2		V
		G = 4, V_I = 3.325 V, V_{CC} = ±15 V	R_L = 50 Ω,	T_A = 25°C	12	13.3		V
				T_A = full range	11.5			V
I_O	Output current drive	G = 4, V_I = 1.025 V, V_{CC} = ±5 V	R_L = 10 Ω,	T_A = 25°C	200	280		mA
		G = 4, V_I = 3.325 V, V_{CC} = ±15 V	R_L = 25 Ω,	T_A = 25°C	360	440		mA
r_o	Output resistance		open loop	T_A = 25°C		14		Ω

electrical characteristics over recommended operating free-air temperature range, T_A = 25°C, V_{CC} = ±15 V, R_F = 750 Ω, R_L = 100 Ω (unless otherwise noted) (continued)

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Quiescent current (per channel)	V_{CC} = ±5V	T_A = 25°C		7.2	9	mA
			T_A = full range			10	
		V_{CC} = ±15 V	T_A = 25°C		8.4	10.5	
			T_A = full range			11.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V ±1 V	T_A = 25°C	53	60		dB
			T_A = full range	50			
		V_{CC} = ±15 V ±1 V	T_A = 25°C	68	73		
			T_A = full range	66			

shutdown characteristics (THS3125 only)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Shutdown quiescent current (per channel)	GND = 0 V V_{CC} = ±5 V to ±15 V	$V_{(SHDN)}$ = 3.3 V		370	500	µA
t_{DIS}	Disable time (see Note 3)				200		ns
t_{EN}	Enable time (see Note 3)				500		ns
$I_{IL(SHDN)}$	Shutdown pin low level leakage current		$V_{(SHDN)}$ = 0 V		18	25	µA
$I_{IH(SHDN)}$	Shutdown pin high level leakage current		$V_{(SHDN)}$ = 3.3 V		110	130	µA

NOTE 3: Disable/enable time is defined as the time from when the shutdown signal is applied to the SHDN pin to when the supply current has reached half of its final value.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Small signal closed loop gain	vs Frequency	1 − 10
	Small and large signal output	vs Frequency	11, 12
	Harmonic distortion	vs Frequency	13, 14, 15
		vs Peak−to−peak output voltage	16, 17
V_n, I_n	Voltage noise and current noise	vs Frequency	18
CMRR	Common-mode rejection ratio	vs Frequency	19
	Crosstalk	vs Frequency	20
Z_o	Output impedance	vs Frequency	21
SR	Slew rate	vs Output voltage step	22
V_{IO}	Input offset voltage	vs Free-air temperature	23
		vs Common-mode input voltage	24
I_B	Input bias current	vs Free-air temperature	25
V_O	Output voltage	vs Load current	26
	Quiescent current	vs Free-air temperature	27
		vs Supply voltage	28
I_{CC}	Shutdown supply current	vs Free-air temperature	29
	Differential gain and phase error	vs 75 Ω serially terminated loads	30, 31
	Shutdown response		32
	Small signal pulse response		33, 34
	Large signal pulse response		35, 36

TYPICAL CHARACTERISTICS

SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY

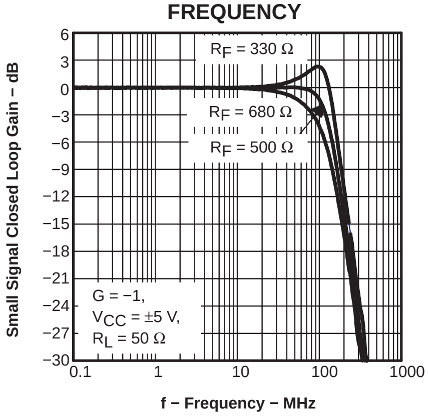


Figure 1

SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY

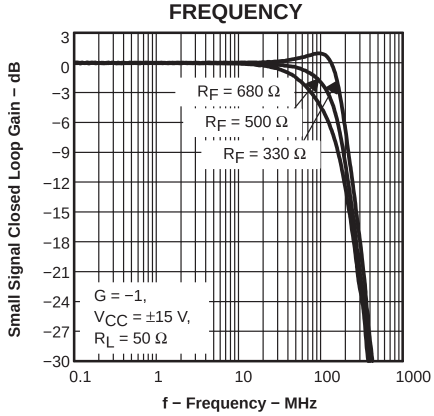


Figure 2

SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY

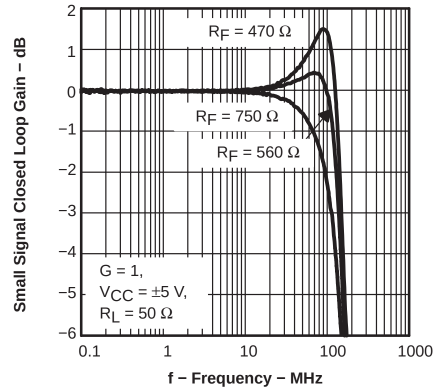


Figure 3

SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY

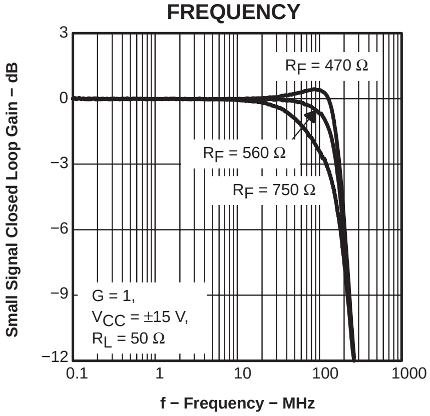


Figure 4

SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY

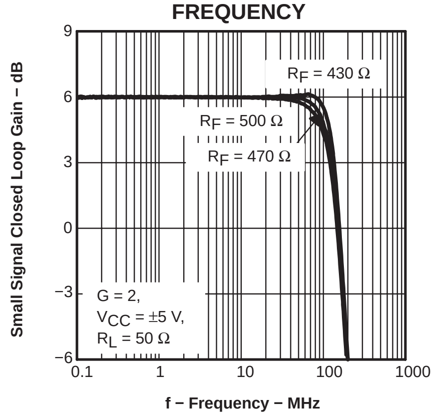


Figure 5

SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY

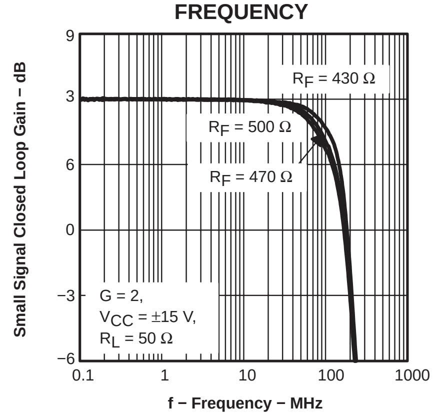


Figure 6

SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY

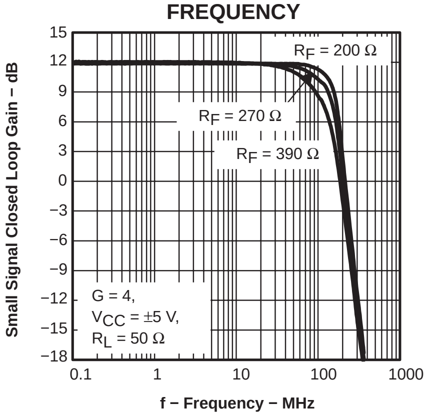


Figure 7

SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY

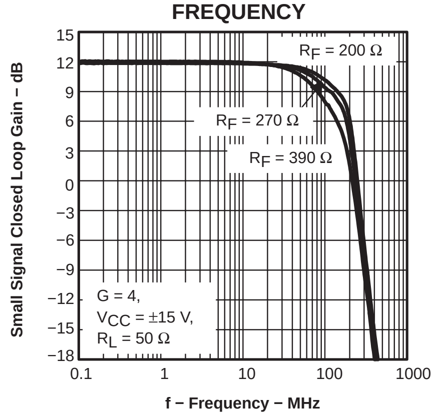


Figure 8

SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY

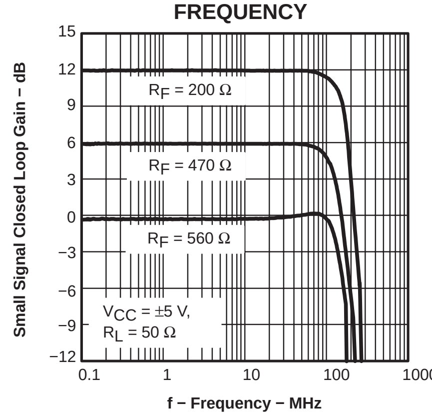


Figure 9

TYPICAL CHARACTERISTICS

SMALL SIGNAL CLOSED LOOP GAIN vs FREQUENCY

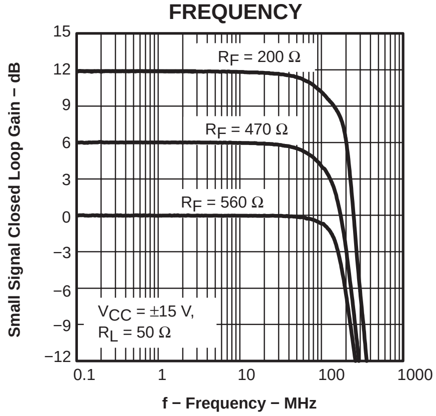


Figure 10

SMALL AND LARGE SIGNAL OUTPUT vs FREQUENCY

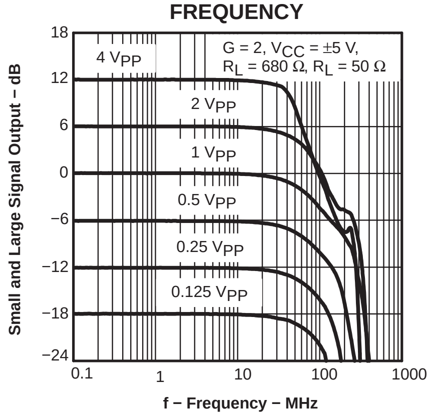


Figure 11

SMALL AND LARGE SIGNAL OUTPUT vs FREQUENCY

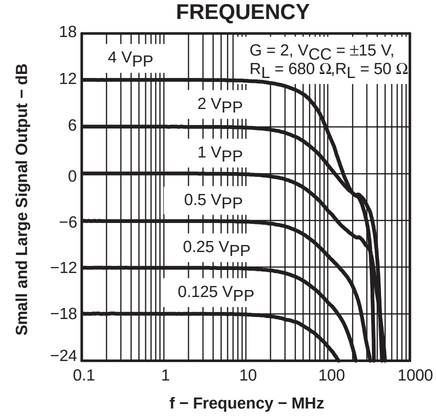


Figure 12

HARMONIC DISTORTION vs FREQUENCY

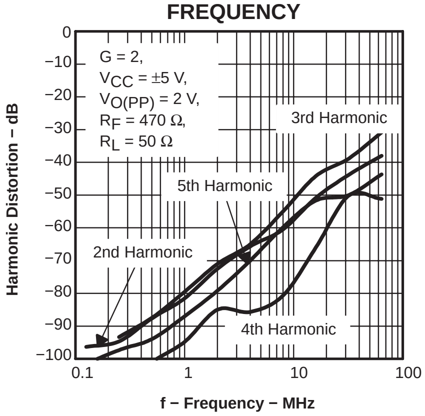


Figure 13

HARMONIC DISTORTION vs FREQUENCY

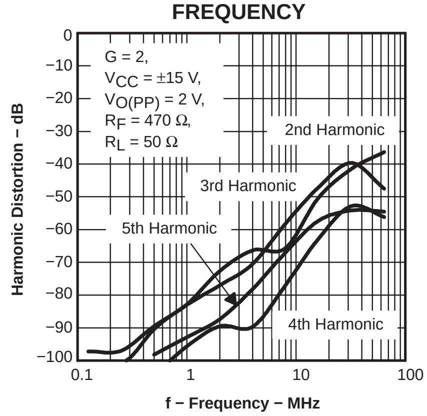


Figure 14

HARMONIC DISTORTION vs FREQUENCY

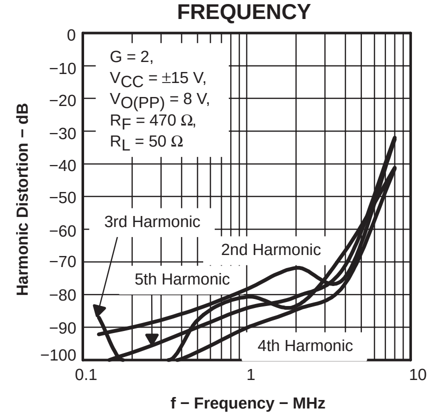


Figure 15

HARMONIC DISTORTION vs PEAK-TO-PEAK OUTPUT VOLTAGE

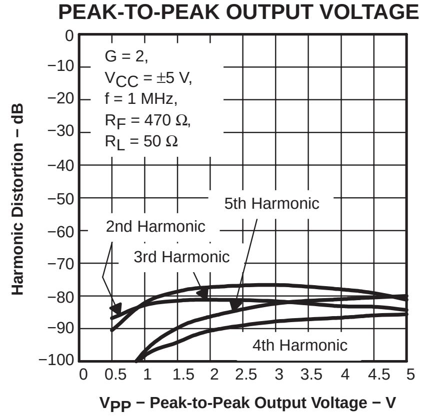


Figure 16

HARMONIC DISTORTION vs PEAK-TO-PEAK OUTPUT VOLTAGE

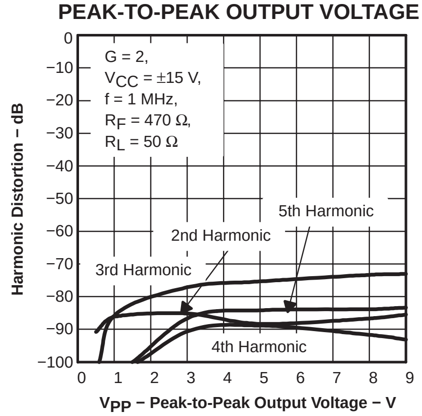


Figure 17

VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY

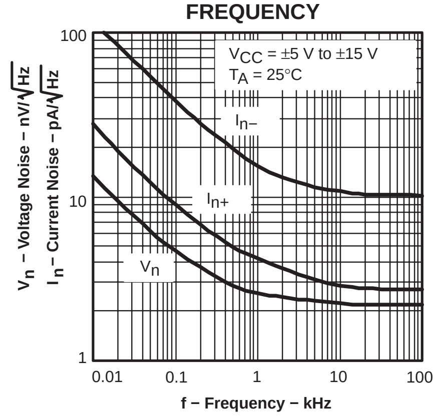


Figure 18

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREQUENCY

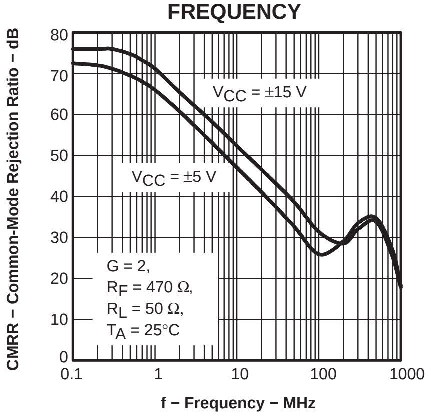


Figure 19

CROSSTALK vs FREQUENCY

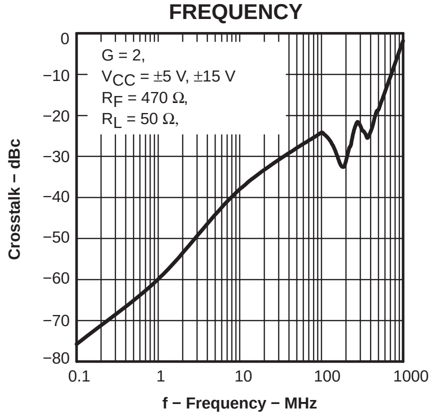


Figure 20

OUTPUT IMPEDANCE vs FREQUENCY

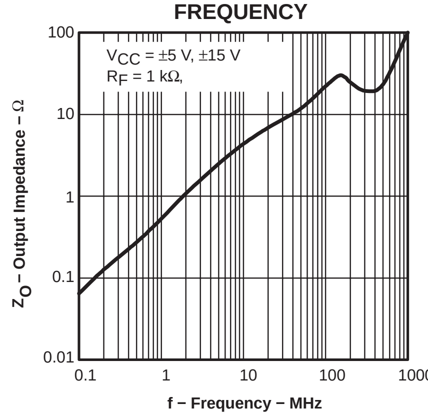


Figure 21

SLEW RATE vs OUTPUT VOLTAGE STEP

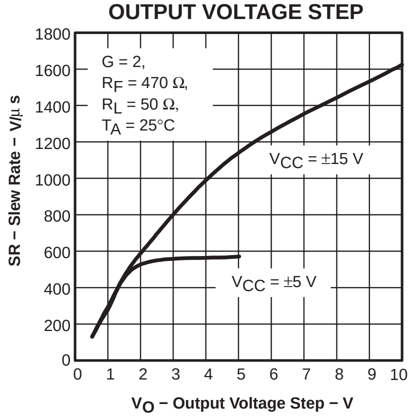


Figure 22

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

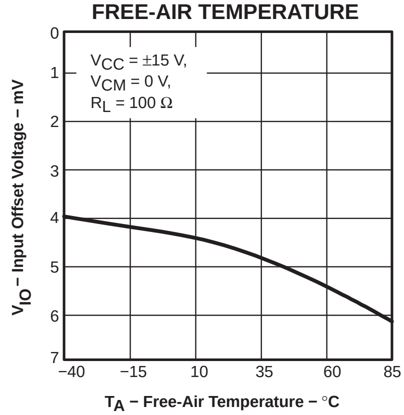


Figure 23

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

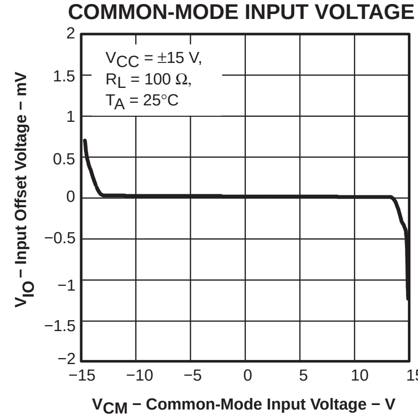


Figure 24

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

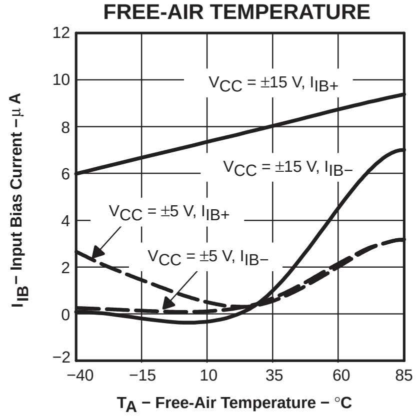


Figure 25

OUTPUT VOLTAGE vs LOAD CURRENT

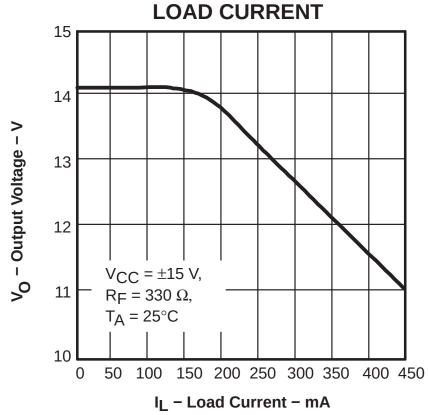


Figure 26

QUIESCENT CURRENT vs FREE-AIR TEMPERATURE

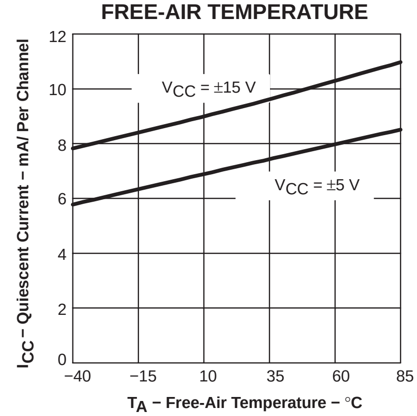


Figure 27

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT vs SUPPLY VOLTAGE

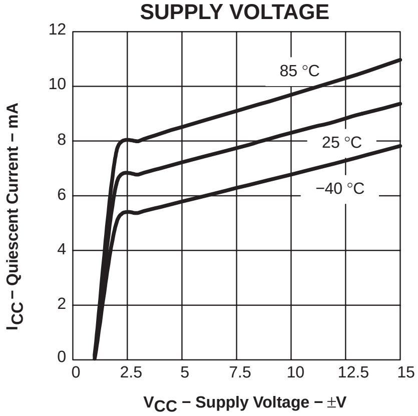


Figure 28

SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE

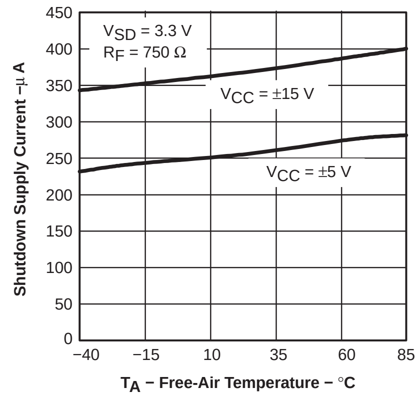


Figure 29

DIFFERENTIAL PHASE AND GAIN ERROR vs 75 Ω SERIALLY TERMINATED LOADS

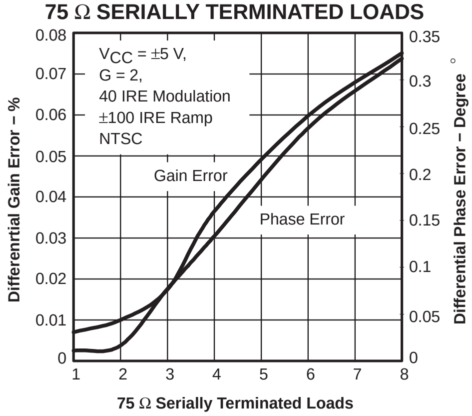


Figure 30

DIFFERENTIAL PHASE AND GAIN ERROR vs 75 Ω SERIALLY TERMINATED LOADS

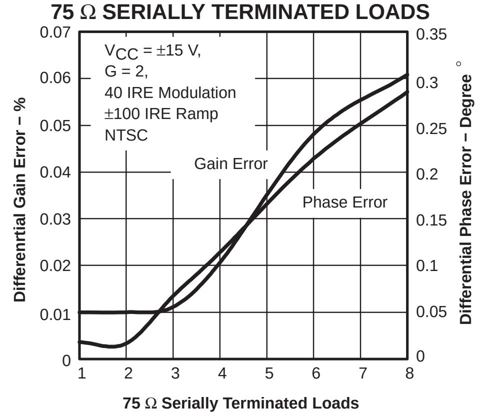


Figure 31

THS3125
SHUTDOWN RESPONSE

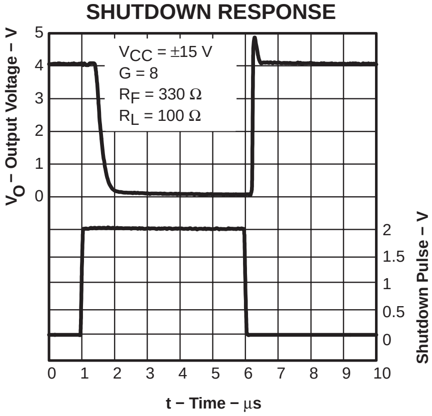


Figure 32

SMALL SIGNAL PULSE RESPONSE

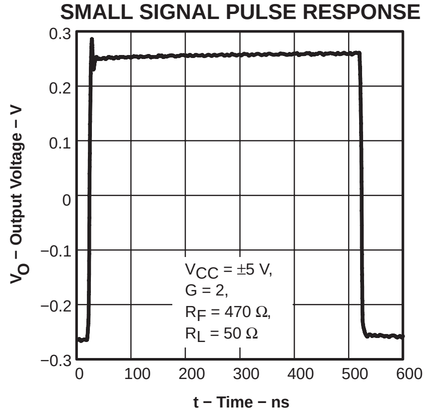


Figure 33

SMALL SIGNAL PULSE RESPONSE

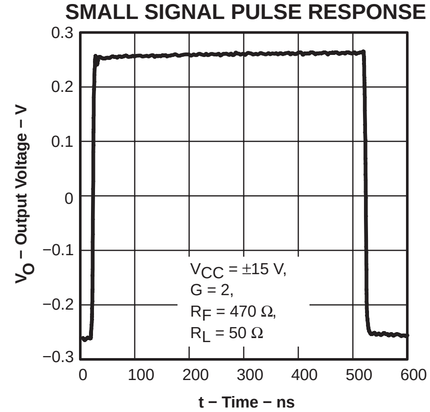


Figure 34

TYPICAL CHARACTERISTICS

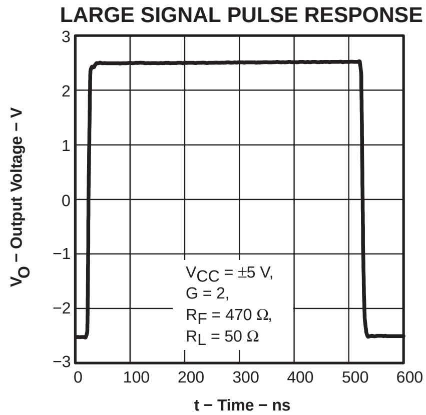


Figure 35

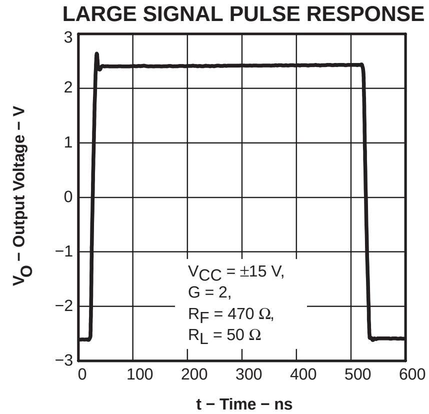


Figure 36

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
THS3122CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3122CDDA	ACTIVE	SO Power PAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS3122CDDAG3	ACTIVE	SO Power PAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS3122CDDAR	ACTIVE	SO Power PAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS3122CDDARG3	ACTIVE	SO Power PAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS3122CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3122CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3122CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3122ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3122IDDA	ACTIVE	SO Power PAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS3122IDDAG3	ACTIVE	SO Power PAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS3122IDDAR	ACTIVE	SO Power PAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS3122IDDARG3	ACTIVE	SO Power PAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
THS3122IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3125CPWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS3125CPWPG4	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS3125ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3125IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3125IPWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS3125IPWPG4	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS3125IPWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
THS3125IPWPRG4	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS &	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						no Sb/Br)		

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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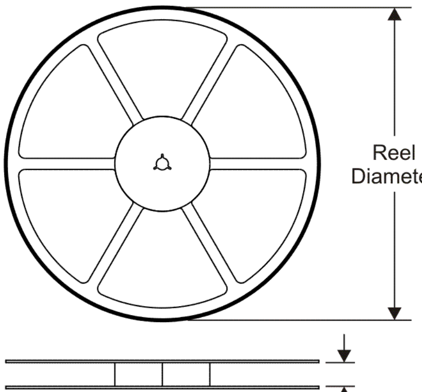
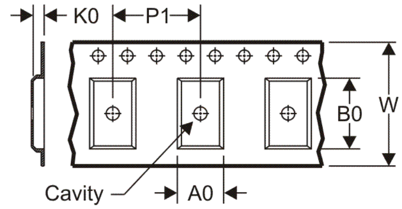
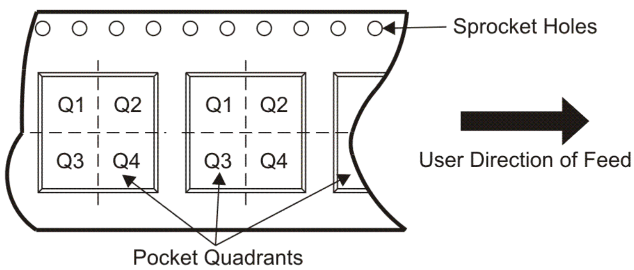
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





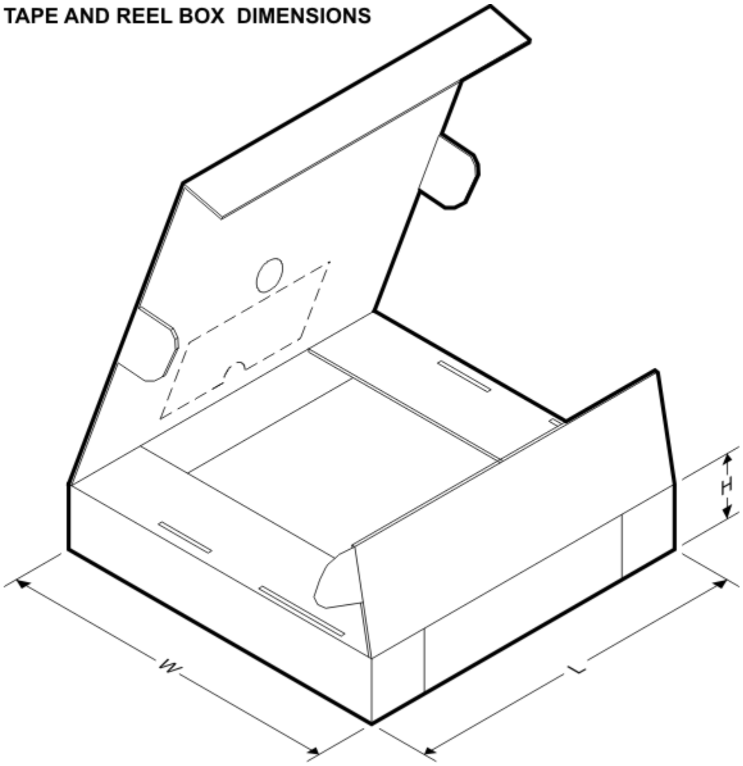
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3122CDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS3122CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS3122IDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS3125IPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.67	5.4	1.6	8.0	12.0	Q1

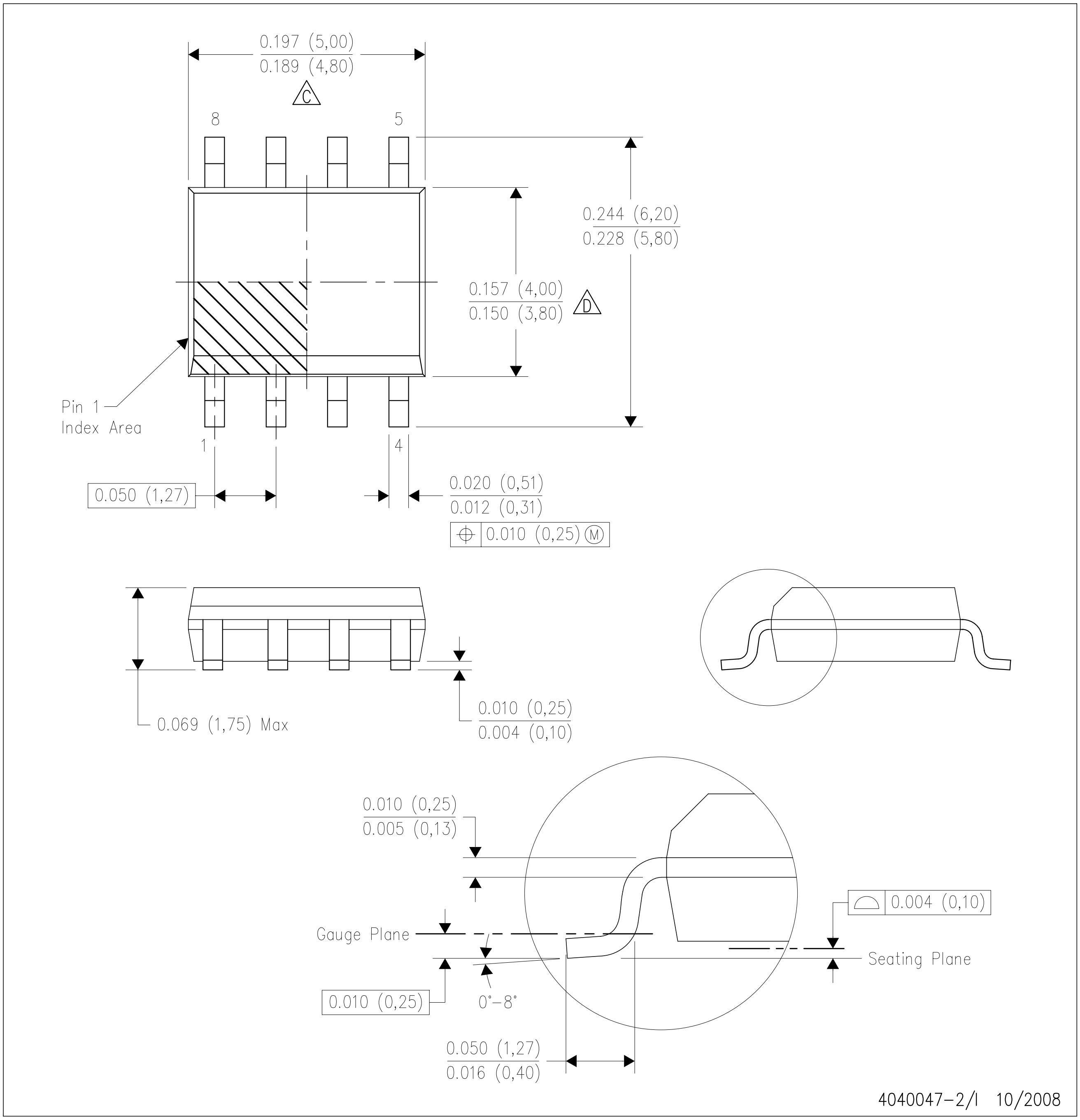
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

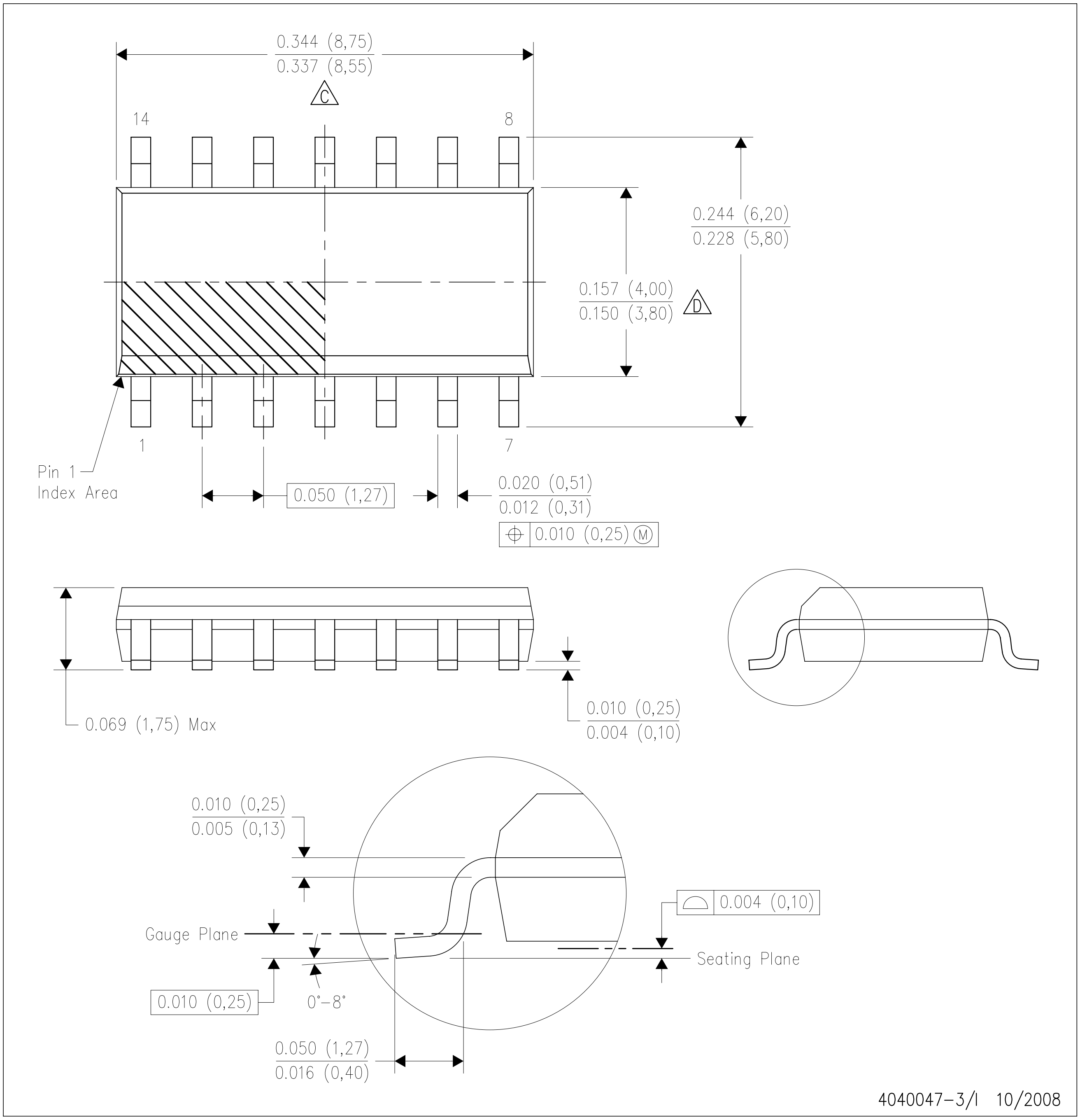
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3122CDDAR	SO PowerPAD	DDA	8	2500	346.0	346.0	29.0
THS3122CDR	SOIC	D	8	2500	346.0	346.0	29.0
THS3122IDDAR	SO PowerPAD	DDA	8	2500	346.0	346.0	29.0
THS3125IPWPR	HTSSOP	PWP	14	2000	346.0	346.0	29.0

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



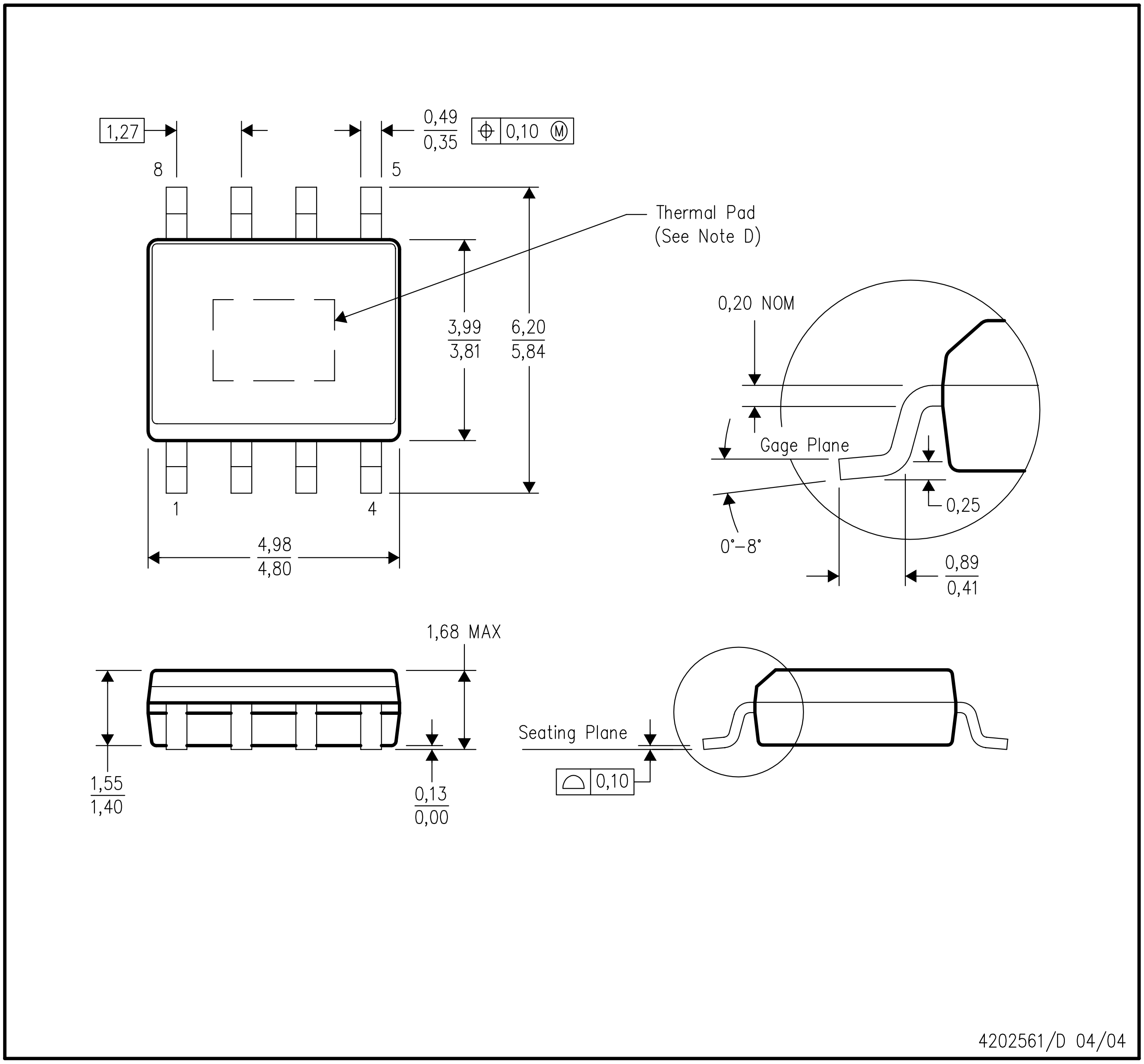
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



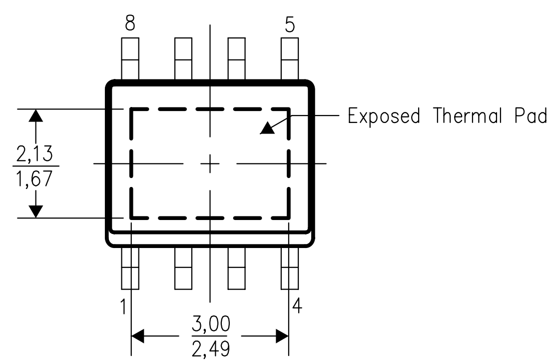
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

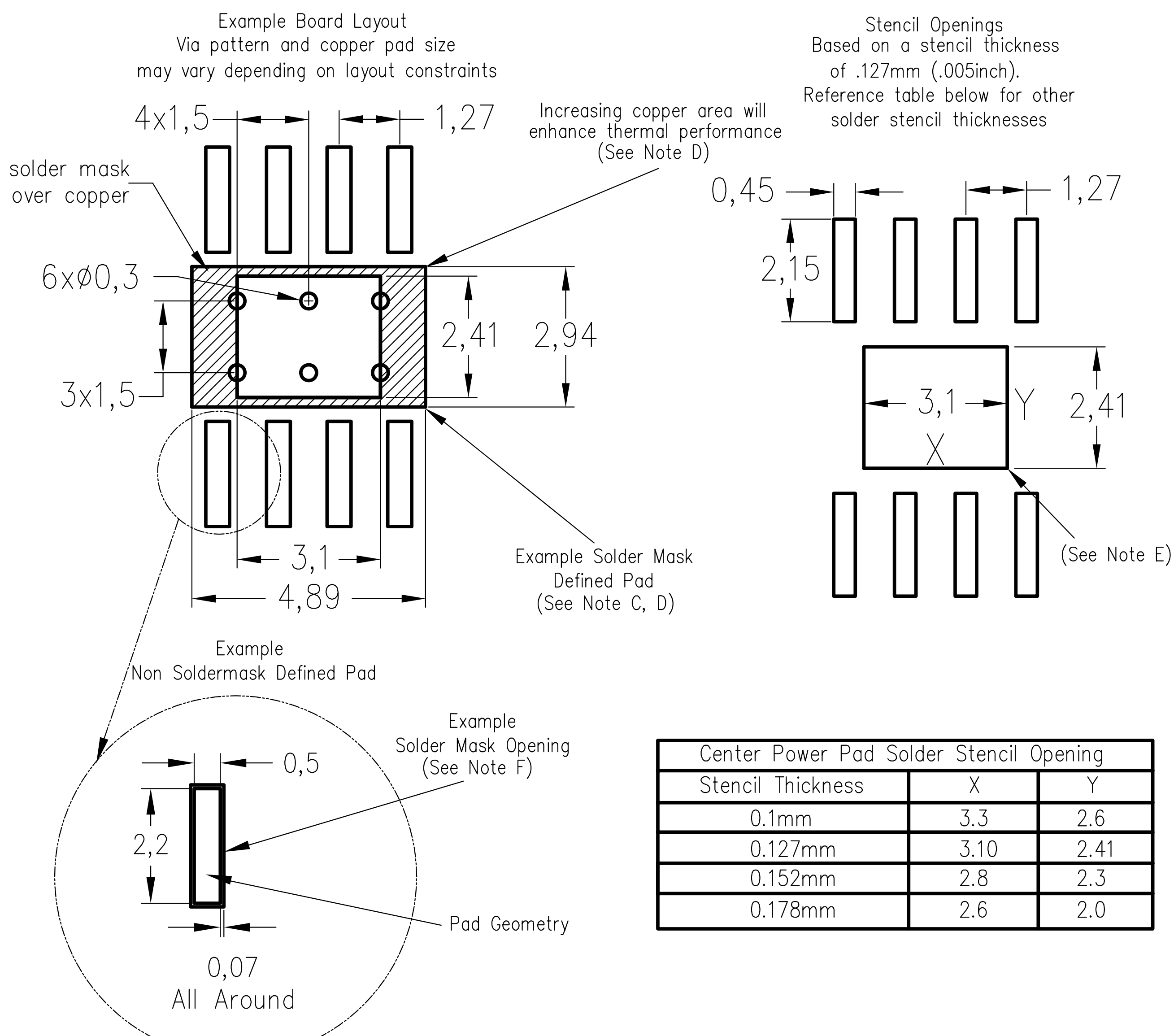


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DDA (R–PDSO–G8) PowerPAD™



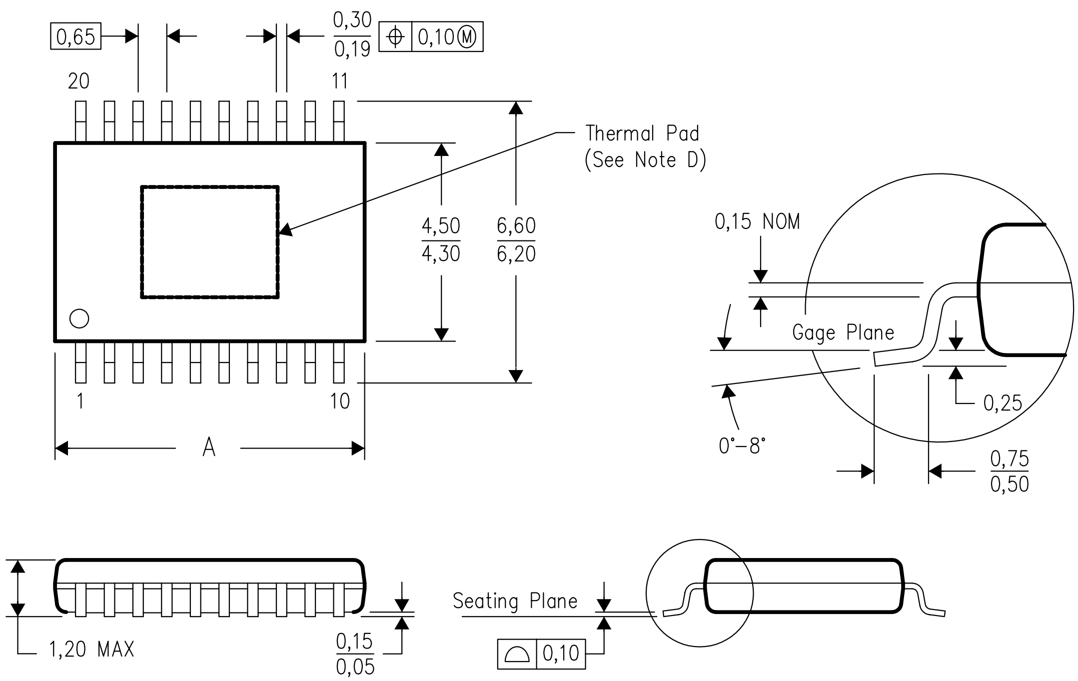
Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.10	2.41
0.152mm	2.8	2.3
0.178mm	2.6	2.0

4208951–4/A 08/07

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

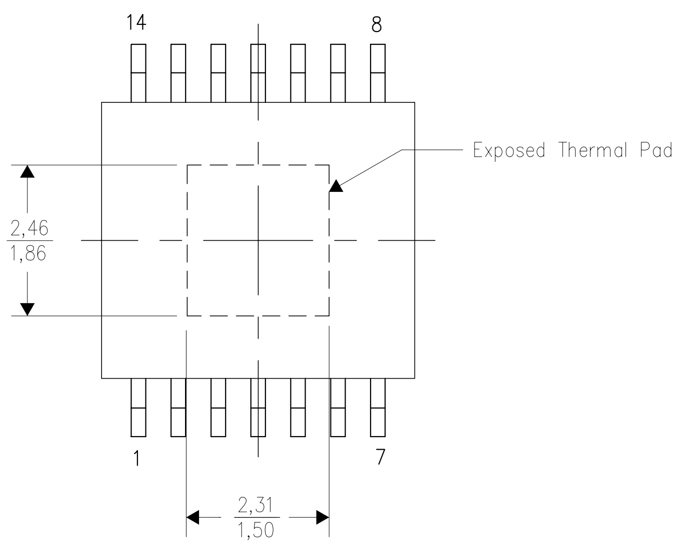
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MO-153

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

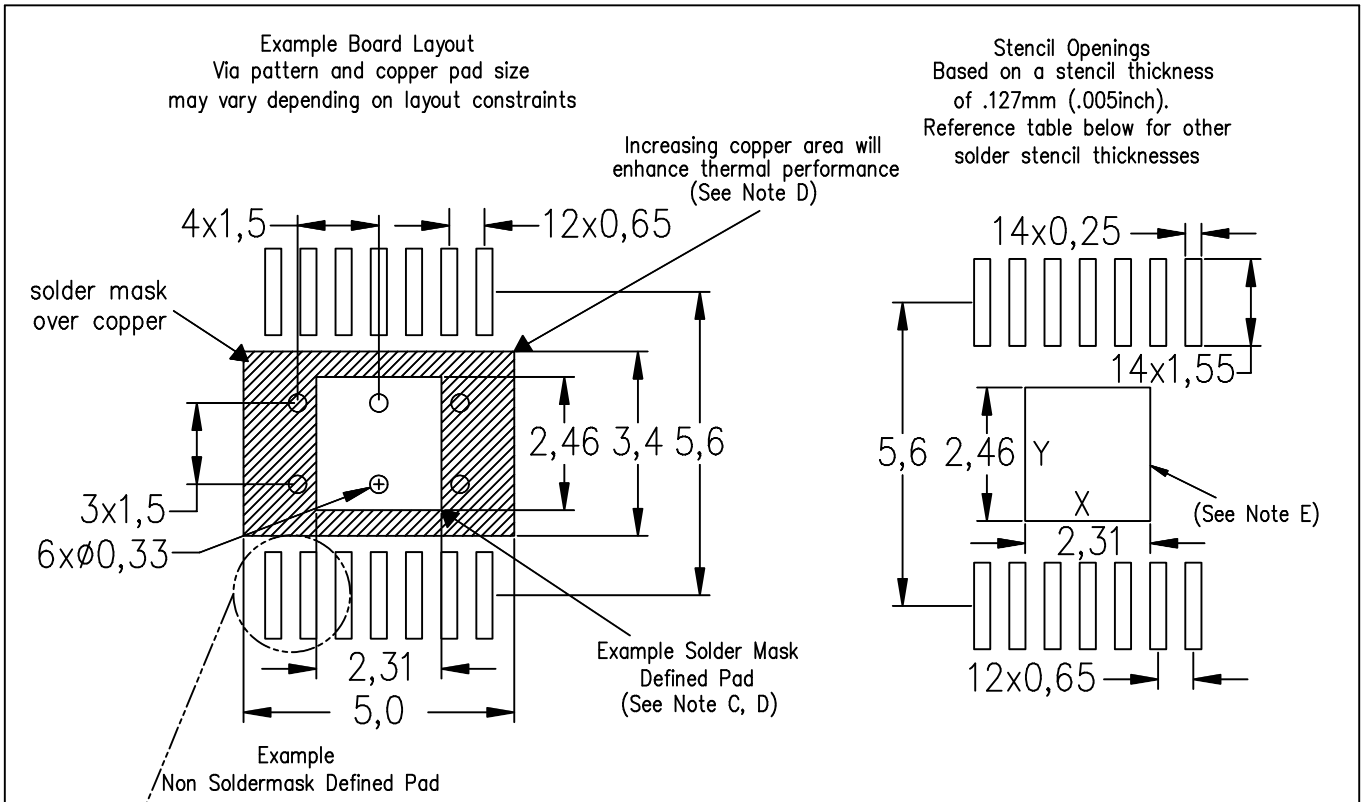


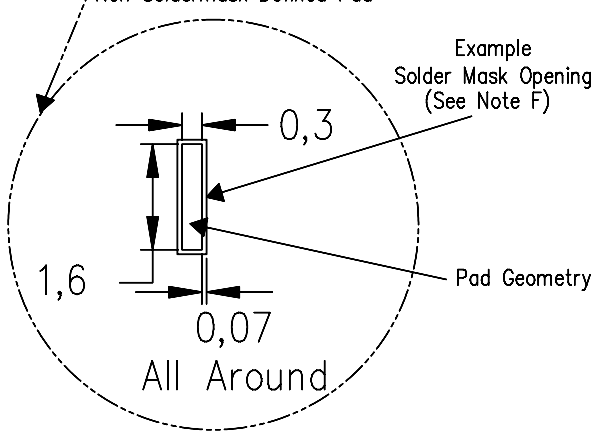
Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G14) PowerPAD™





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/F 11/08

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.