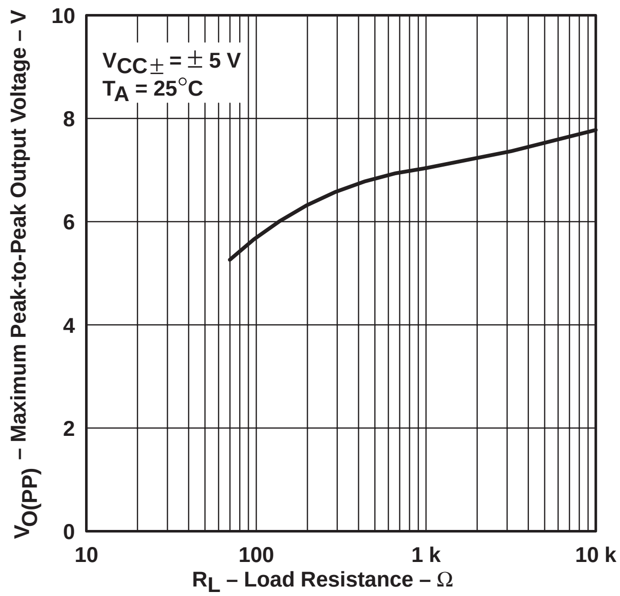
- **Excellent Output Drive Capability**
  V_O = ± 2.5 V Min at R_L = 100 Ω, $V_{CC\pm}$ = ± 5 V
  V_O = ± 12.5 V Min at R_L = 600 Ω, $V_{CC\pm}$ = ± 15 V
- **Low Supply Current . . . 280 μA Typ**
- **Decompensated for High Slew Rate and Gain-Bandwidth Product**
  A_{VD} = 0.5 Min
  Slew Rate = 10 V/μs Typ
  Gain-Bandwidth Product = 6.5 MHz Typ
- **Wide Operating Supply Voltage Range**
  $V_{CC\pm}$ = ± 3.5 V to ± 18 V
- **High Open-Loop Gain . . . 280 V/mV Typ**
- **Low Offset Voltage . . . 500 μV Max**
- **Low Offset Voltage Drift With Time**
  0.04 μV/Month Typ
- **Low Input Bias Current . . . 5 pA Typ**

description

The TLE2161, TLE2161A, and TLE2161B are JFET-input, low-power, precision operational amplifiers manufactured using the Texas Instruments Excalibur process. Decompensated for stability with a minimum closed-loop gain of 5, these devices combine outstanding output drive capability with low power consumption, excellent dc precision, and high gain-bandwidth product.

In addition to maintaining the traditional JFET advantages of fast slew rates and low input bias and offset currents, the Excalibur process offers outstanding parametric stability over time and temperature. This results in a device that remains precise even with changes in temperature and over years of use.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV 1.5 mV 3 mV	— TLE2161ACD TLE2161CD	— —	— —	TLE2161BCP TLE2161ACP TLE2161CP
–40°C to 85°C	500 μV 1.5 mV 3 mV	— TLE2161AID TLE2161ID	— —	— —	TLE2161BIP TLE2161AIP TLE2161IP
–55°C to 125°C	500 μV 1.5 mV 3 mV	— TLE2161AMD TLE2161MD	— TLE2161AMFK TLE2161MFK	TLE2161BMJG TLE2161AMJG TLE2161MJG	TLE2161BMP TLE2161AMP TLE2161MP

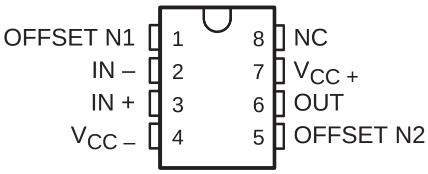
The D packages are available taped and reeled. Add R suffix to device type (e.g., TLE2161ACDR).

description (continued)

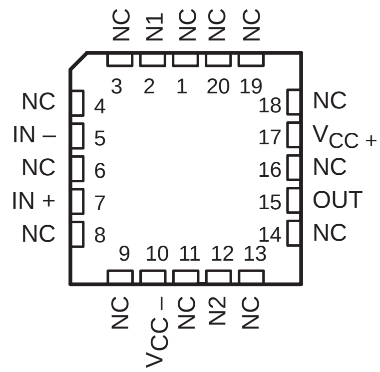
A variety of available options includes small-outline packages and chip-carrier versions for high-density system applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C.

D, JG, OR P PACKAGE
(TOP VIEW)

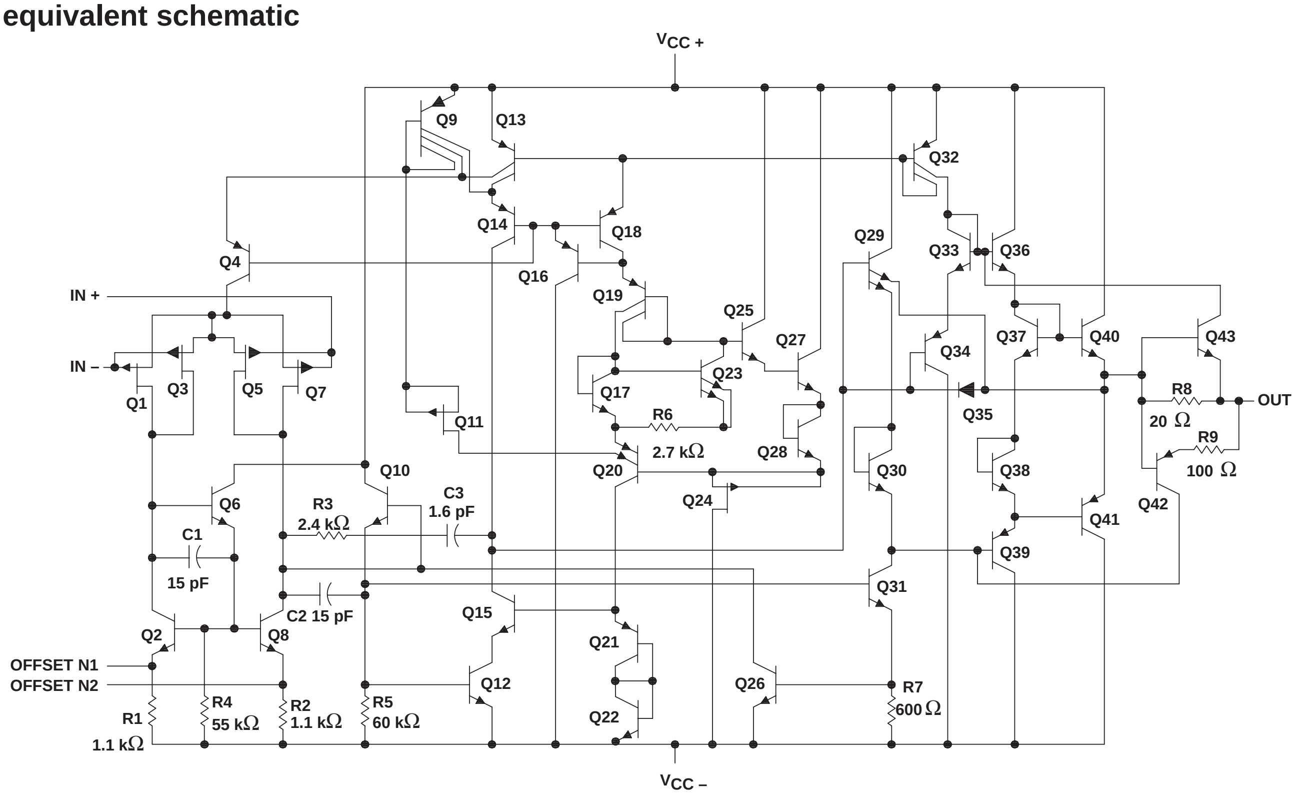


FK PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic



All component values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) . . . . . 19 V
Supply voltage, V_{CC-} . . . . . – 19 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ± 38 V
Input voltage range, V_I (any input) . . . . . $V_{CC\pm}$
Input current, I_I (each input) . . . . . ± 1 mA
Output current, I_O . . . . . ± 80 mA
Total current into V_{CC+} . . . . . 80 mA
Total current out of V_{CC-} . . . . . 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . – 40°C to 85°C
M suffix . . . . . – 55°C to 125°C
Storage temperature range, T_{stg} . . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60seconds: JG package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+}, and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The output may be shorted to either supply. Temperature and /or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC\pm}$		±3.5	±18	±3.5	±18	+3.5	±18	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	–1.6	4	–1.6	4	–1.6	4	V
	$V_{CC\pm} = \pm 15$ V	–11	13	–11	13	–11	13	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161C, TLE2161AC TLE2161BC			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2161C	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.8	3.1	mV
				Full range			4	
		TLE2161AC		25°C		0.6	2.6	
				Full range			3.5	
		TLE2161BC		25°C		0.5	1.9	
				Full range			2.4	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			0.8	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			2	nA
V_{ICR}	Common-mode input voltage range			25°C	–1.6 to 4	–2 to 6		V
				Full range	–1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3.3			
			$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	–3.7	–3.9		V
				Full range	–3.3			
			$R_L = 100\ \Omega$	25°C	–2.5	–2.7		
				Full range	–2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
			$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_O = 0$ to –2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	75			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		280	325	μA
				Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		29		μA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2161C, TLE2161AC TLE2161BC MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		59	100	nV/√Hz
		R_S = 20 Ω, f = 1 kHz			43	60	
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 5, f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		5.8		MHz
		f = 100 kHz, R_L = 100 kΩ, C_L = 100 pF			4.3		
t_s	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ	25°C		420		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C		70°		
		A_{VD} = 5, R_L = 100 Ω, C_L = 100 pF			84°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm$ 15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161C, TLE2161AC TLE2161BC MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161C	V_{IC} = 0, R_S = 50 Ω	25°C		0.6	3	mV
				Full range			3.9	
		TLE2161AC		25°C		0.5	1.5	
				Full range			2.5	
		TLE2161BC		25°C		0.3	0.5	
				Full range			1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			1	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			3	nA
V_{ICR}	Common-mode input voltage range			25°C	–11 to 13	–12 to 16		V
				Full range	–11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		R_L = 10 kΩ	25°C	13.2	13.7		V
				Full range	13			
			R_L = 600 Ω	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		R_L = 10 kΩ	25°C	–13.2	–13.7		V
				Full range	–13			
			R_L = 600 Ω	25°C	–12.5	–13		
				Full range	–12			
A_{VD}	Large-signal differential voltage amplification		V_O = ±10 V, R_L = 10 kΩ	25°C	30	230		V/mV
				Full range	20			
			V_O = 0 to 8 V, R_L = 600 Ω	25°C	25	100		
				Full range	10			
			V_O = 0 to – 8 V, R_L = 600 Ω	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		I_O = 0	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min, R_S = 50 Ω	25°C	72	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm}$ = ±5 V to ±15 V, RS = 50 Ω	25°C	75	93		dB
				Full range	75			
I_{CC}	Supply current		VO = 0, No load	25°C		290	350	μA
				Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		34		μA

† Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2161C, TLE2161AC TLE2161BC			UNIT
				MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	$A_{VD} = 5$, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20$ Ω, f = 10 Hz	25°C		70	100	nV/√Hz
		$R_S = 20$ Ω, f = 1 kHz			40	60	
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)} = 2$ V, $A_{VD} = 5$, f = 10 kHz, $R_L = 10$ kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		6.4		MHz
		f = 100 kHz, $R_L = 600$ Ω, $C_L = 100$ pF			5.6		
t_s	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 5$, $R_L = 10$ kΩ	25°C		116		kHz
ϕ_m	Phase margin (see Figure 3)	$A_{VD} = 5$, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		72°		
		$A_{VD} = 5$, $R_L = 600$ Ω, $C_L = 100$ pF			78°		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161I, TLE2161AI TLE2161BI			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLE2161I	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.8	3.1	mV
				Full range			4.4	
		TLE2161AI		25°C		0.6	2.6	
				Full range			3.9	
		TLE2161BI		25°C		0.5	1.9	
				Full range			2.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			2	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			4	nA
V_{ICR}	Common-mode input voltage range			25°C	–1.6 to 4	–2 to 6		V
				Full range	–1.6 to 4			
V_{OM+}	Maximum positive peak output voltage		$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3.1			
			$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	–3.7	–3.9		V
				Full range	–3.1			
			$R_L = 100\ \Omega$	25°C	–2.5	–2.7		
				Full range	–2			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
			$V_O = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_O = 0$ to –2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.25			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	65	82		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to $\pm$ 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		280	325	μA
				Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		29		μA

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A= 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2161I, TLE2161AI TLE2161BI			UNIT
				MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	$A_{VD} = 5$, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20$ Ω, f = 10 Hz	25°C		59	100	nV/√Hz
		$R_S = 20$ Ω, f = 1 kHz			43	60	
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)} = 2$ V, $A_{VD} = 5$, f = 10 kHz, $R_L = 10$ kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		5.8		MHz
		f = 100 kHz, $R_L = 100$ Ω, $C_L = 100$ pF			4.3		
t_s	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 5$, $R_L = 10$ kΩ	25°C		420		kHz
ϕ_m	Phase margin (see Figure 3)	$A_{VD} = 5$, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		70°		
		$A_{VD} = 5$, $R_L = 100$ Ω, $C_L = 100$ pF			84°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161I, TLE2161AI TLE2161BI MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161I	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3	mV
				Full range			4.3	
		TLE2161AI		25°C		0.5	1.5	
				Full range			2.9	
		TLE2161BI		25°C		0.3	0.5	
				Full range			1.3	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			3	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			5	nA
V_{ICR}	Common-mode input voltage range			25°C	–11 to 13	–12 to 16		V
				Full range	–11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13.2	13.7		V
				Full range	13			
			$R_L = 600\ \Omega$	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	–13.2	–13.7		V
				Full range	–13			
			$R_L = 600\ \Omega$	25°C	–12.5	–13		
				Full range	–12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
				Full range	20			
			$V_O =$ 0 to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
				Full range	10			
			$V_O =$ 0 to – 8 V, $R_L = 600\ \Omega$	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		290	350	μA
				Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		34		μA

† Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2161I, TLE2161AI TLE2161IB MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	$A_{VD} = 5$, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20$ Ω, f = 10 Hz	25°C		70	100	nV/√Hz
		$R_S = 20$ Ω, f = 1 kHz			40	60	
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)} = 2$ V, $A_{VD} = 5$, f = 10 kHz, $R_L = 10$ kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		6.4		MHz
		f = 100 kHz, $R_L = 600$ Ω, $C_L = 100$ pF			5.6		
t_s	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 5$, $R_L = 10$ kΩ	25°C		116		kHz
ϕ_m	Phase margin (see Figure 3)	$A_{VD} = 5$, $R_L = 10$ kΩ, $C_L = 100$ pF	25°C		72°		
		$A_{VD} = 5$, $R_L = 600$ Ω, $C_L = 100$ pF			78°		

† Full range is – 40°C to 85°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161M TLE2161AM TLE2161BM MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.8	3.1	mV
				Full range			6	
		TLE2161AM		25°C		0.6	2.6	
				Full range			4.6	
		TLE2161BM		25°C		0.5	1.9	
				Full range			3.1	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		1		pA
				Full range			15	nA
I_{IB}	Input bias current			25°C		3		pA
				Full range			30	nA
V_{ICR}	Common-mode input voltage range			25°C	–1.6 to 4	–2 to 6		V
				Full range	–1.6 to 4			V
V_{OM+}	Maximum positive peak output voltage swing	All packages	$R_L = 10\ k\Omega$	25°C	3.5	3.7		V
				Full range	3			
		FK and JG packages	$R_L = 600\ \Omega$	25°C	2.5	3.6		V
				Full range	2			
		D and P packages	$R_L = 100\ \Omega$	25°C	2.5	3.1		
				Full range	2			
V_{OM-}	Maximum negative peak output voltage swing	All packages	$R_L = 10\ k\Omega$	25°C	–3.7	–3.9		V
				Full range	–3			
		FK and JG packages	$R_L = 600\ \Omega$	25°C	–2.5	–3.5		
				Full range	–2			
		D and P packages	$R_L = 100\ \Omega$	25°C	–2.5	–2.7		
				Full range	–2			
A_{VD}	Large-signal differential voltage amplification	All packages	$V_0 = \pm 2.8$ V, $R_L = 10\ k\Omega$	25°C	15	80		V/mV
				Full range	2			
		FK and JG packages	$V_0 = 0$ to 2.5 V, $R_L = 600\ \Omega$	25°C	1	65		
				Full range	0.5			
			$V_0 = 0$ to –2.5 V, $R_L = 600\ \Omega$	25°C	1	16		
				Full range	0.5			
		D and P packages	$V_0 = 0$ to 2 V, $R_L = 100\ \Omega$	25°C	0.75	45		
				Full range	0.5			
			$V_0 = 0$ to –2 V, $R_L = 100\ \Omega$	25°C	0.5	3		
				Full range	0.25			

† Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 5$ V (unless otherwise noted continued)

PARAMETER		TEST CONDITIONS	T_A†	TLE2161M TLE2161AM TLE2161BM			UNIT
				MIN	TYP	MAX	
r_i	Input resistance		25°C		10^{12}		Ω
c_i	Input capacitance		25°C		4		pF
z_o	Open-loop output impedance	$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, $R_S = 50\ \Omega$	25°C	65	82		dB
			Full range	60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
			Full range	65			
I_{CC}	Supply current	$V_O = 0$, No load	25°C		280	325	μA
			Full range			350	
ΔI_{CC}	Supply-current change over operating temperature range		Full range		39		μA

† Full range is – 55°C to 125°C.

operating characteristics, $V_{CC\pm} = \pm 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TLE2161M TLE2161AM TLE2161BM			UNIT
			MIN	TYP	MAX	
SR	Slew rate (see Figure 1)	$A_{VD} = 5$, $R_L = 10$ kΩ, $C_L = 100$ pF		10		V/μs
V_n	Equivalent input noise voltage (see Figure 2)	$R_S = 20\ \Omega$, f = 10 Hz		59		nV/√Hz
		$R_S = 20\ \Omega$, f = 1 kHz		43		
$V_{n(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		1.1		μV
I_n	Equivalent input noise current	f = 1 kHz		1		fA/√Hz
THD	Total harmonic distortion	$A_{VD} = 5$, $V_{O(PP)} = 2$ V, f = 10 kHz, $R_L = 10$ kΩ		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, $R_L = 10$ kΩ, $C_L = 100$ pF		5.8		MHz
		f = 100 kHz, $R_L = 600$ kΩ, $C_L = 100$ pF		4.3		
t_s	Settling time	ε = 0.1%		5		μs
		ε = 0.01%		10		
B_{OM}	Maximum output-swing bandwidth	$A_{VD} = 5$, $R_L = 10$ kΩ		420		kHz
ϕ_m	Phase margin (see Figure 3)	$A_{VD} = 5$, $R_L = 10$ kΩ, $C_L = 100$ pF		70°		
		$A_{VD} = 5$, $R_L = 600\ \Omega$, $C_L = 100$ pF		84°		

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLE2161M TLE2161AM TLE2161BM MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLE2161M	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.6	3	mV
				Full range			6	
		TLE2161AM		25°C		0.5	1.5	
				Full range			3.6	
		TLE2161BM		25°C		0.3	0.5	
				Full range			1.7	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		6		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.04		μV/mo
I_{IO}	Input offset current			25°C		2		pA
				Full range			20	nA
I_{IB}	Input bias current			25°C		4		pA
				Full range			40	nA
V_{ICR}	Common-mode input voltage range			25°C	–11 to 13	–12 to 16		V
				Full range	–11 to 13			V
V_{OM+}	Maximum positive peak output voltage swing		$R_L = 10\ k\Omega$	25°C	13.2	13.7		V
				Full range	12.5			
			$R_L = 600\ \Omega$	25°C	12.5	13.2		
				Full range	12			
V_{OM-}	Maximum negative peak output voltage swing		$R_L = 10\ k\Omega$	25°C	–13.2	–13.7		V
				Full range	–12.5			
			$R_L = 600\ \Omega$	25°C	–12.5	–13		
				Full range	–12			
A_{VD}	Large-signal differential voltage amplification		$V_O = \pm 10$ V, $R_L = 10\ k\Omega$	25°C	30	230		V/mV
				Full range	20			
			$V_O = 0$ to 8 V, $R_L = 600\ \Omega$	25°C	25	100		
				Full range	7			
			$V_O = 0$ to – 8 V, $R_L = 600\ \Omega$	25°C	3	25		
				Full range	1			
r_i	Input resistance			25°C		10^{12}		Ω
c_i	Input capacitance			25°C		4		pF
z_o	Open-loop output impedance		$I_O = 0$	25°C		280		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}min$, $R_S = 50\ \Omega$	25°C	72	90		dB
				Full range	65			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm} / \Delta V_{IO}$)		$V_{CC\pm} = \pm 5$ V to ± 15 V, $R_S = 50\ \Omega$	25°C	75	93		dB
				Full range	65			
I_{CC}	Supply current		$V_O = 0$, No load	25°C		290	350	μA
				Full range			375	
ΔI_{CC}	Supply-current change over operating temperature range			Full range		46		μA

† Full range is – 55°C to 125°C.

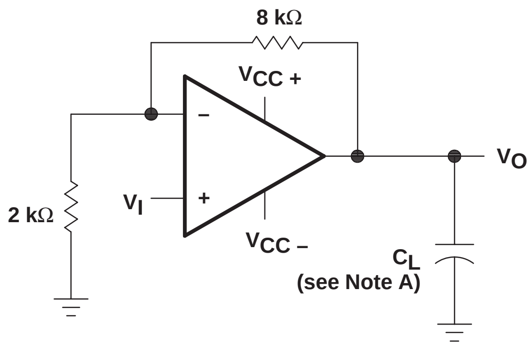
NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLE2161M TLE2161AM TLE2161BM MIN	TYP	MAX	UNIT
SR	Slew rate (see Figure 1)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C	7	10		V/μs
			Full range	5			
V_n	Equivalent input noise voltage (see Figure 2)	R_S = 20 Ω, f = 10 Hz	25°C		70		nV/√Hz
		R_S = 20 Ω, f = 1 kHz			40		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	25°C		1.1		μV
I_n	Equivalent input noise current	f = 1 Hz	25°C		1.1		fA/√Hz
THD	Total harmonic distortion	$V_{O(PP)}$ = 2 V, A_{VD} = 5, f = 10 kHz, R_L = 10 kΩ	25°C		0.025%		
	Gain-bandwidth product (see Figure 3)	f = 100 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		6.4		MHz
		f = 100 kHz, R_L = 600 Ω, C_L = 100 pF			5.6		
t_s	Settling time	ε = 0.1%	25°C		5		μs
		ε = 0.01%			10		
B_{OM}	Maximum output-swing bandwidth	A_{VD} = 5, R_L = 10 kΩ	25°C		116		kHz
ϕ_m	Phase margin (see Figure 3)	A_{VD} = 5, R_L = 10 kΩ, C_L = 100 pF	25°C		72°		
		A_{VD} = 5, R_L = 600 Ω, C_L = 100 pF			78°		

† Full range is – 55°C to 125°C.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

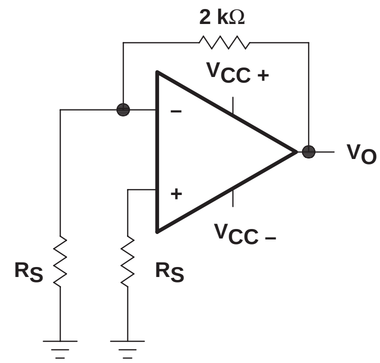
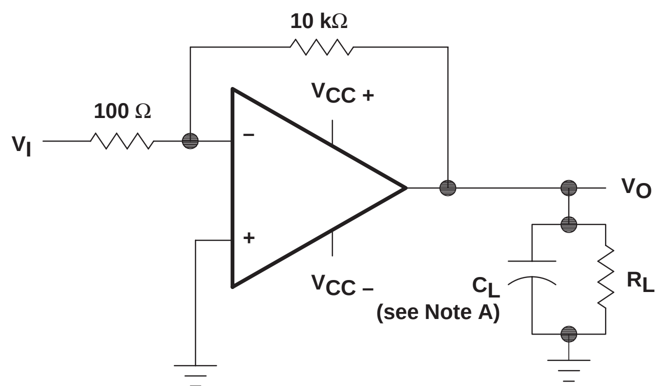


Figure 2. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Gain-Bandwidth Product and Phase-Margin Test Circuit

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

Input bias and offset current

At the picoampere bias-current level typical of the TLE2161, TLE2161A, and TLE2161B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket, and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	4
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	5 6
I_{IO}	Input offset current	vs Free-air temperature	6
V_{ICR}	Common-mode input voltage range limits	vs Free-air temperature	7
V_{OM}	Maximum positive peak output voltage	vs Output current	8
V_{OM}	Maximum negative peak output voltage	vs Output current	9
V_{OM}	Maximum peak output voltage	vs Supply voltage	10, 11, 12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13, 14, 15
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	16 17
I_{OS}	Short-circuit output current	vs Elapsed time	18
	Large-signal voltage amplification	vs Free-air temperature	19
z_o	Output impedance	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
I_{CC}	Supply current	vs Supply voltage vs Free-air temperature	22 23
	Pulse response	Small signal Large signal	24, 25 26, 27
	Noise voltage (referred to input)	0.1 to 10 Hz	28
V_n	Equivalent input noise voltage	vs Frequency	29
THD	Total harmonic distortion	vs Frequency	30, 31
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	32 33
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature	34 35
	Phase shift	vs Frequency	16

TYPICAL CHARACTERISTICS†

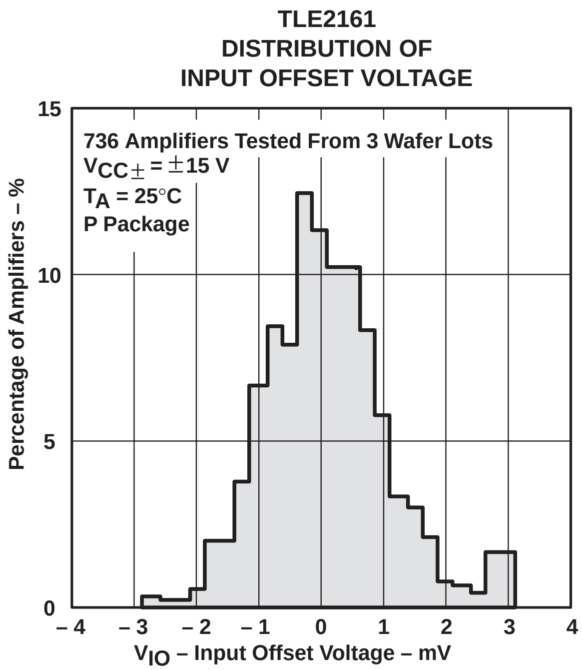


Figure 4

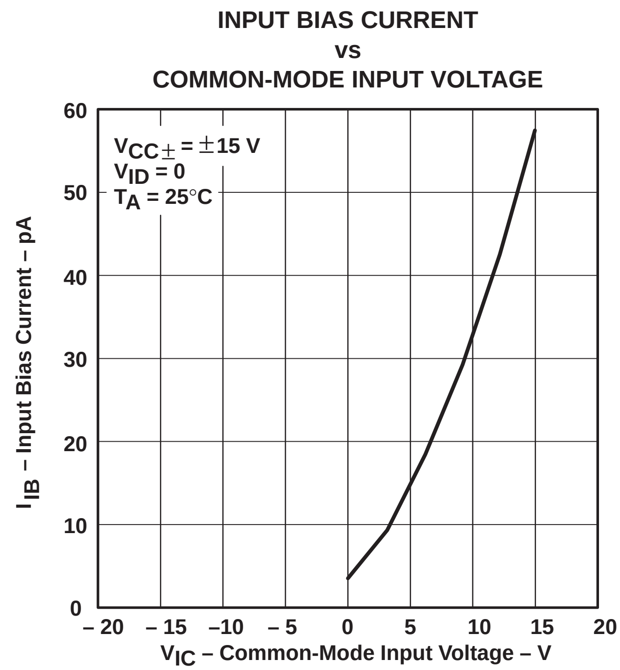


Figure 5

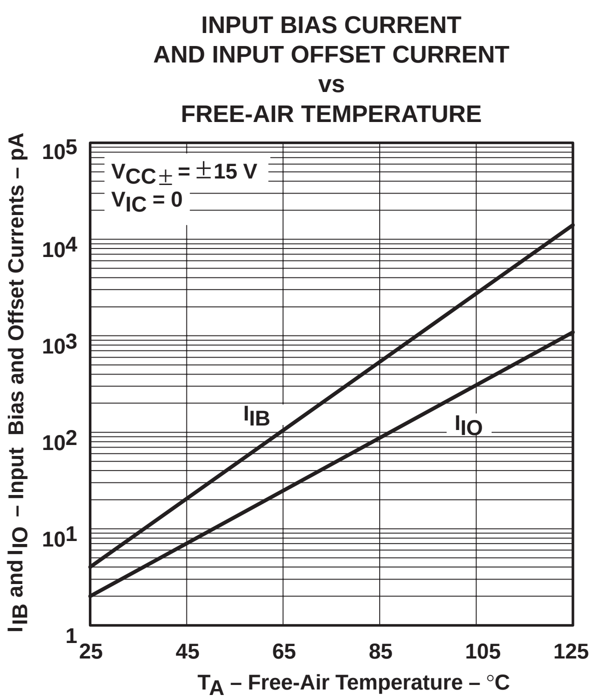


Figure 6

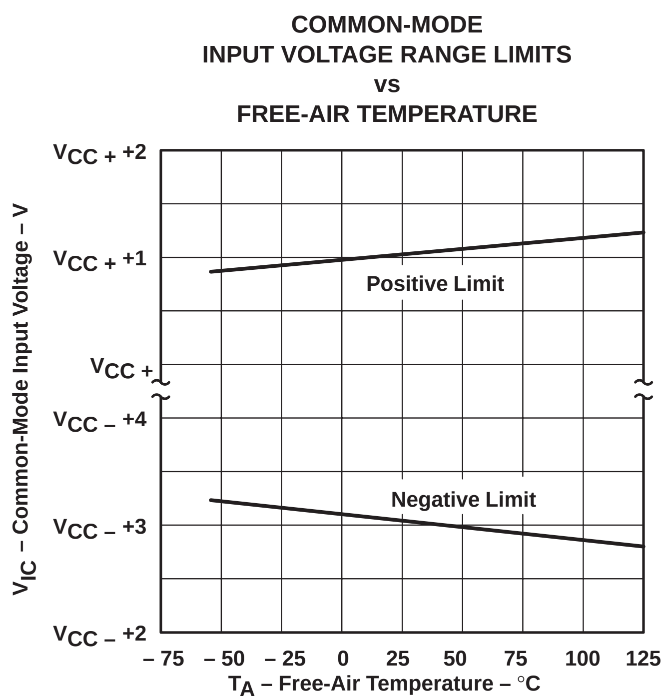


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

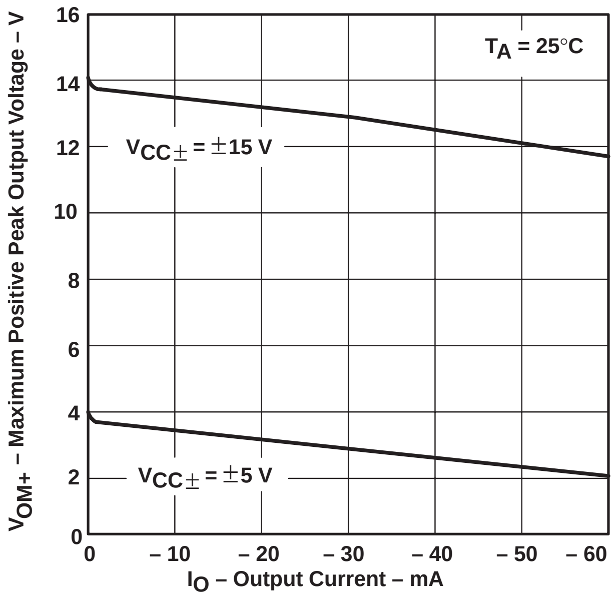


Figure 8

MAXIMUM NEGATIVE PEAK
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

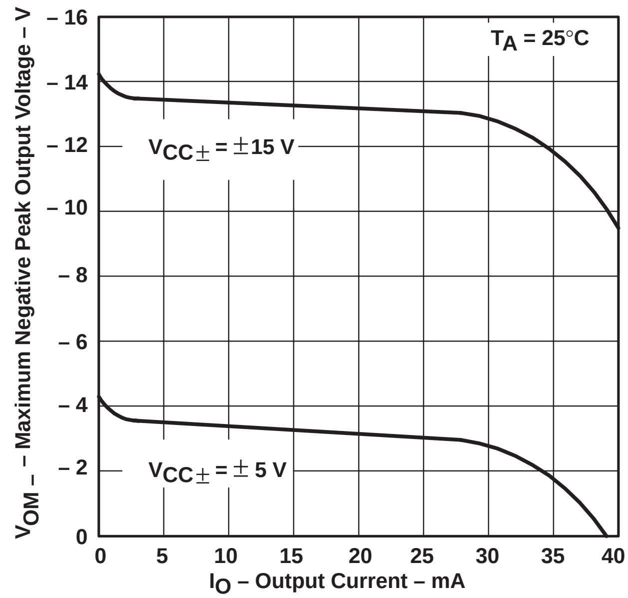


Figure 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

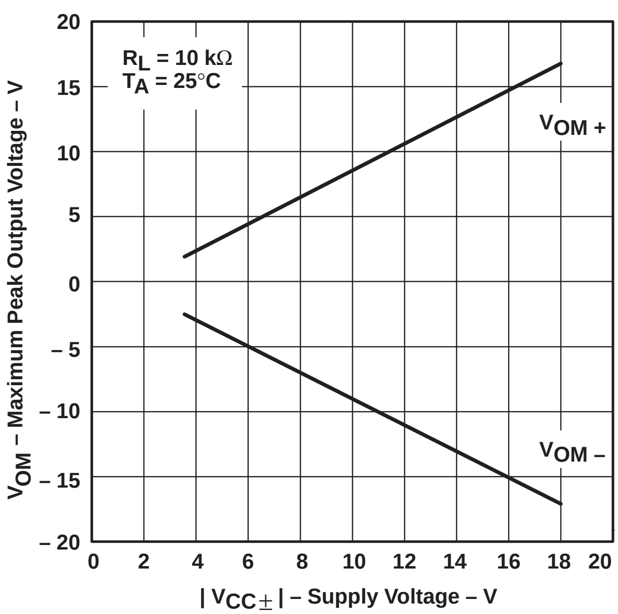


Figure 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

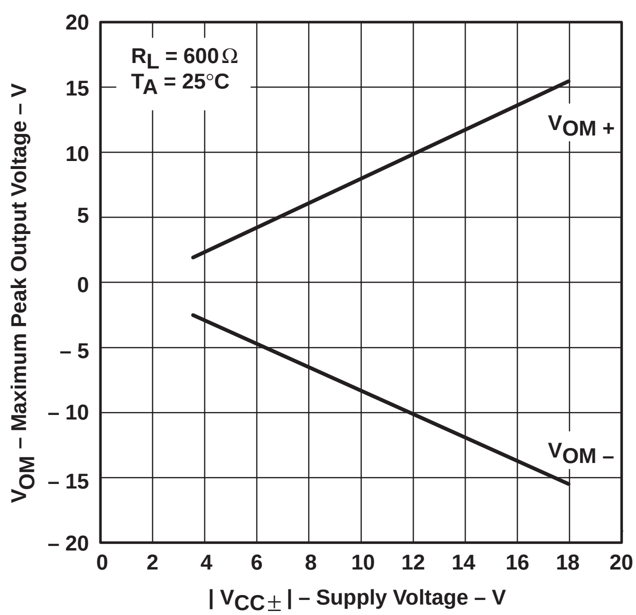


Figure 11

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

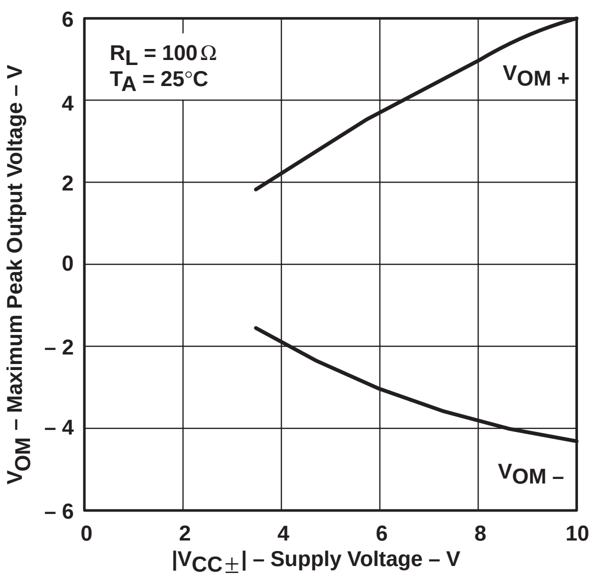


Figure 12

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

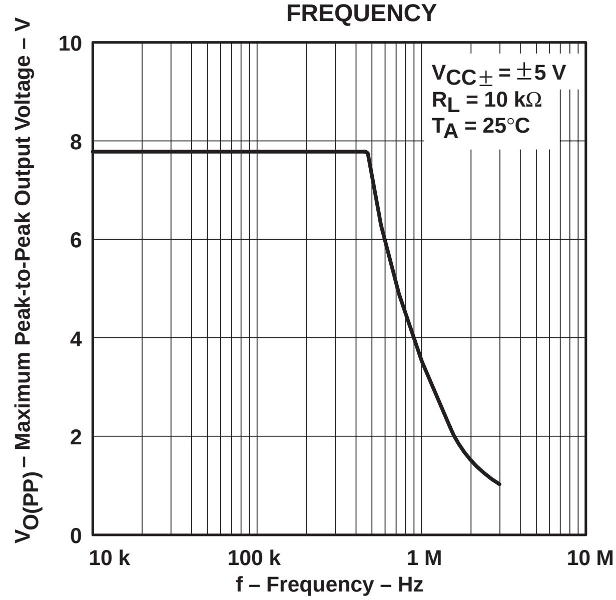


Figure 13

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FRQUENCY

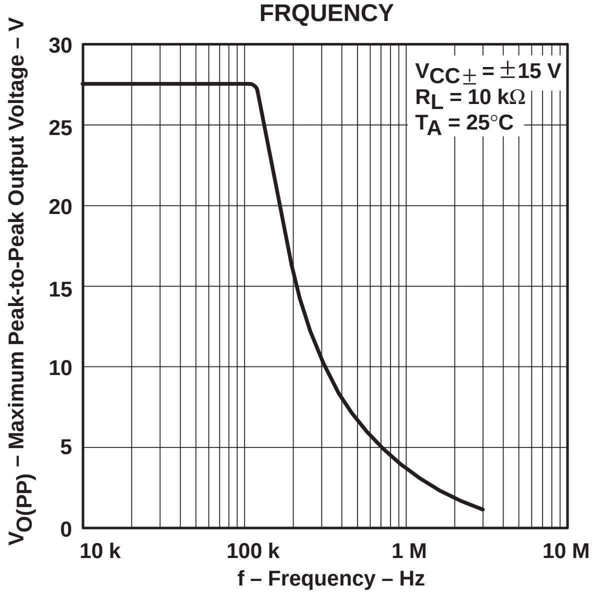


Figure 14

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

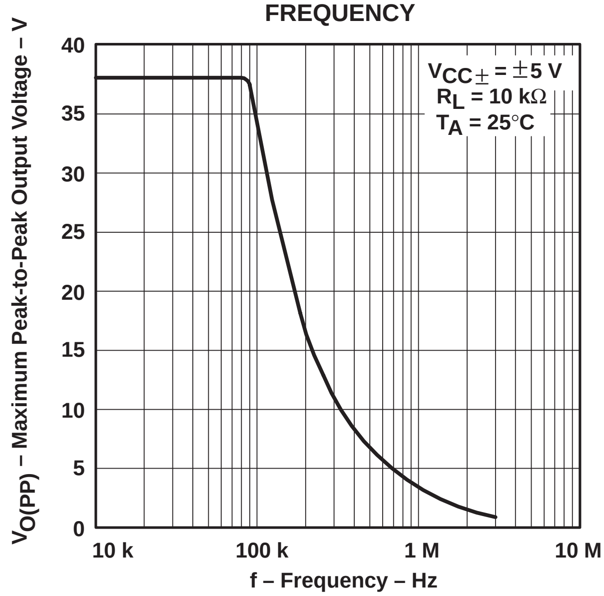


Figure 15

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FRQUENCY

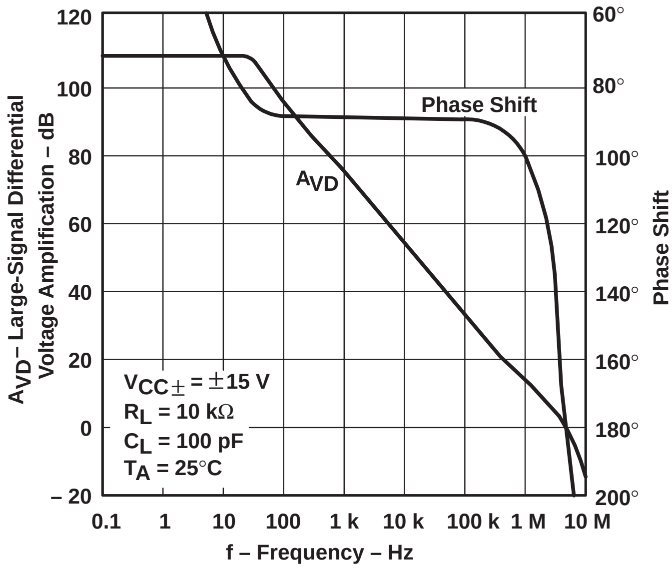


Figure 16

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

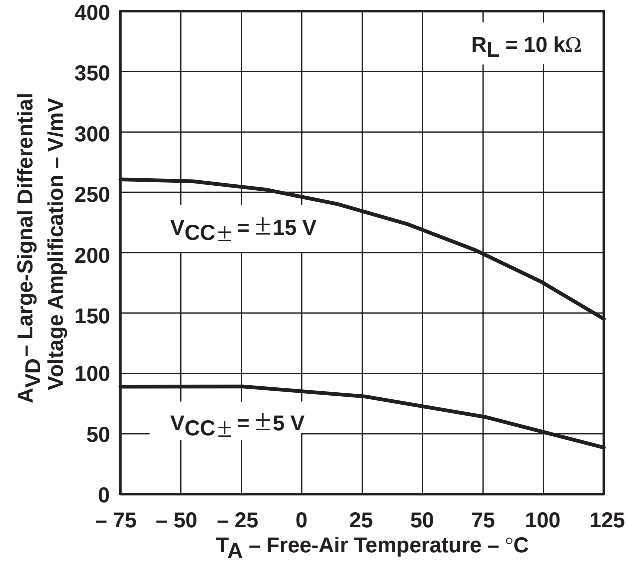


Figure 17

SHORT-CIRCUIT OUTPUT CURRENT vs ELAPSED TIME

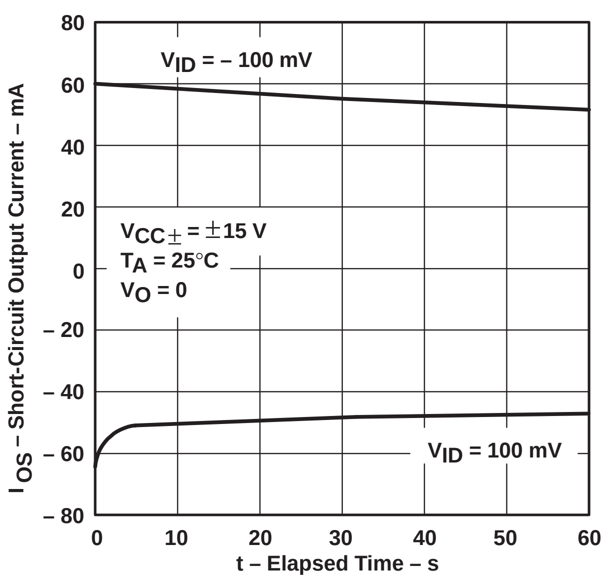


Figure 18

LARGE-SIGNAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

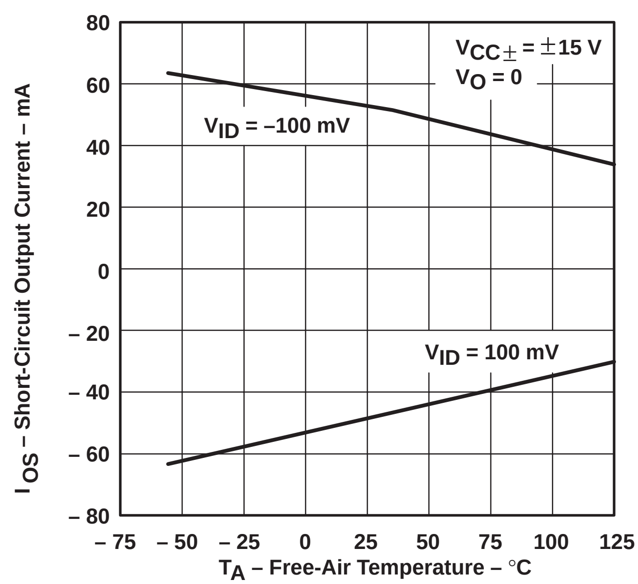


Figure 19

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OUTPUT IMPEDANCE vs FREQUENCY

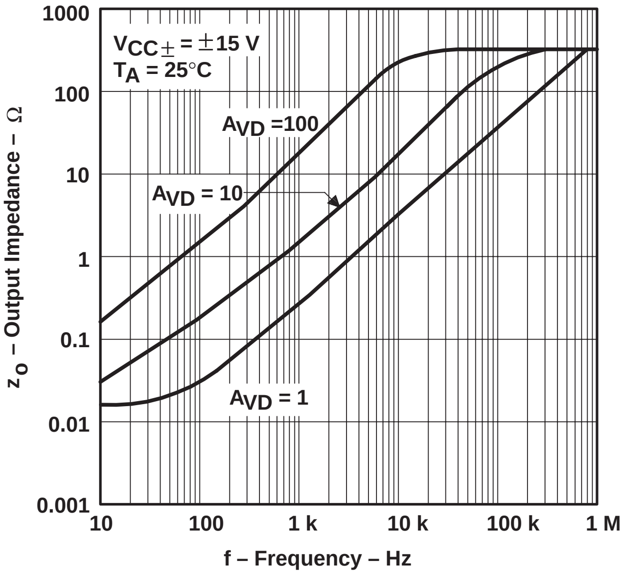


Figure 20

COMMON-MODE REJECTION RATIO vs FREQUENCY

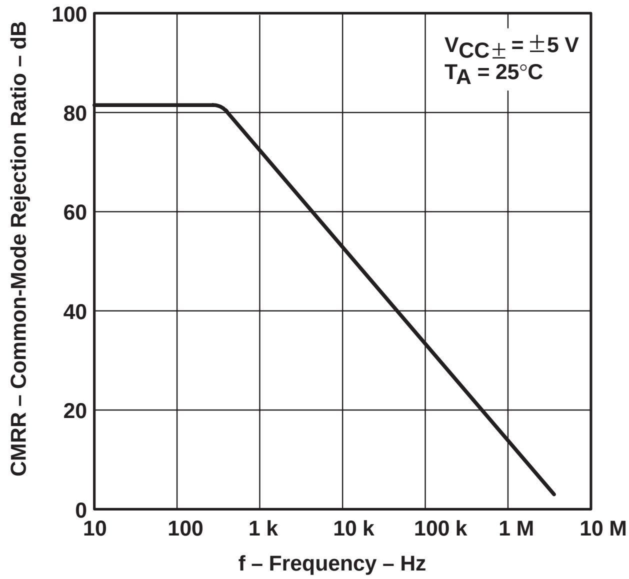


Figure 21

SUPPLY CURRENT vs SUPPLY VOLTAGE

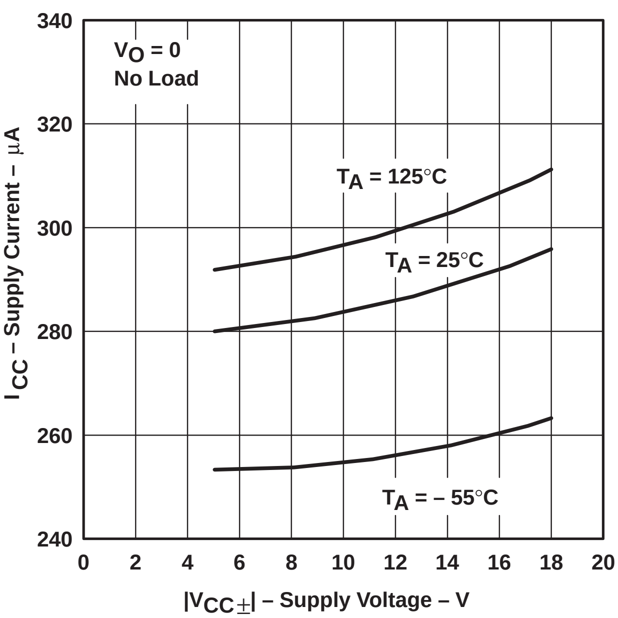


Figure 22

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

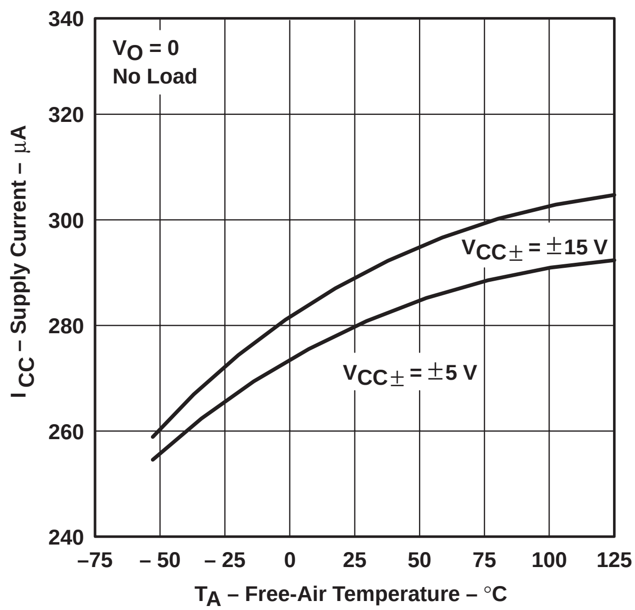


Figure 23

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

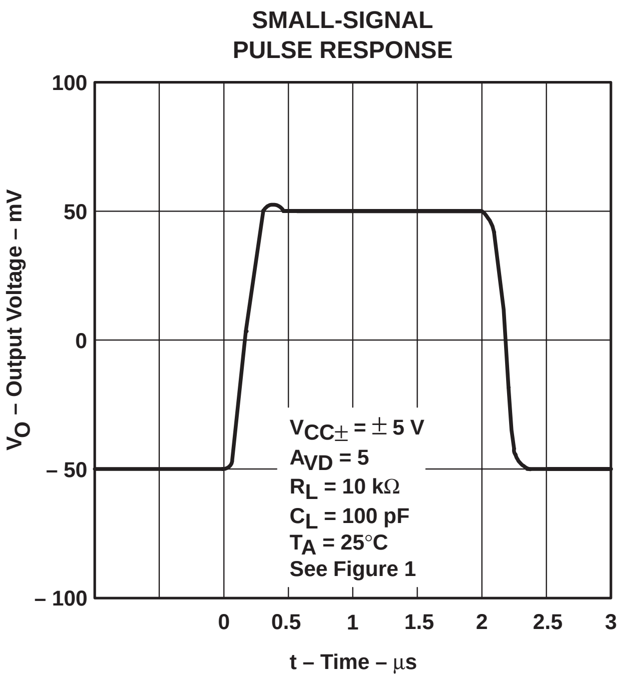


Figure 24

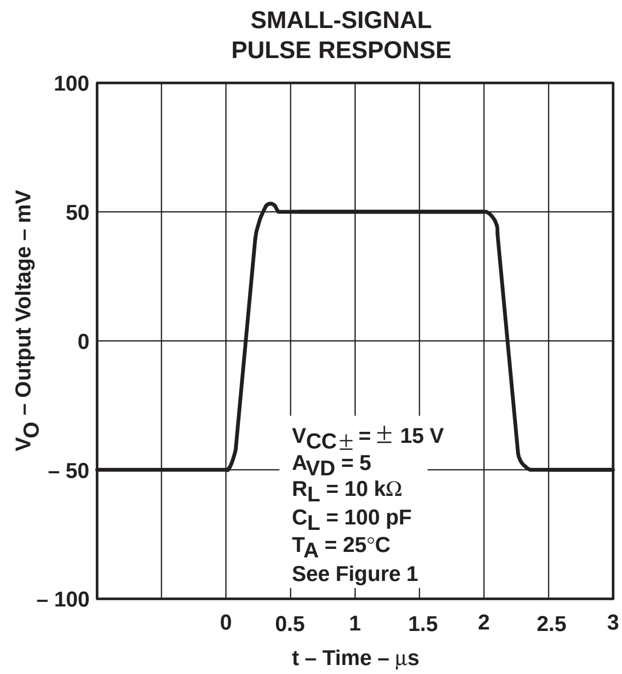


Figure 25

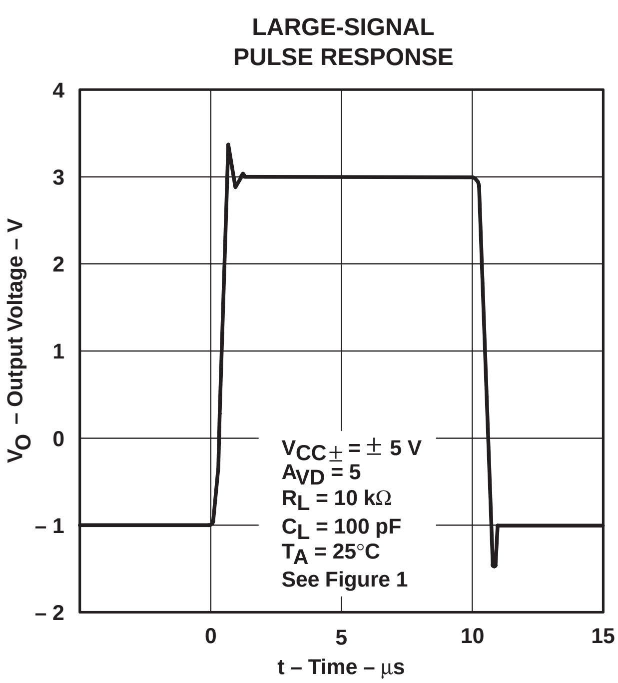


Figure 26

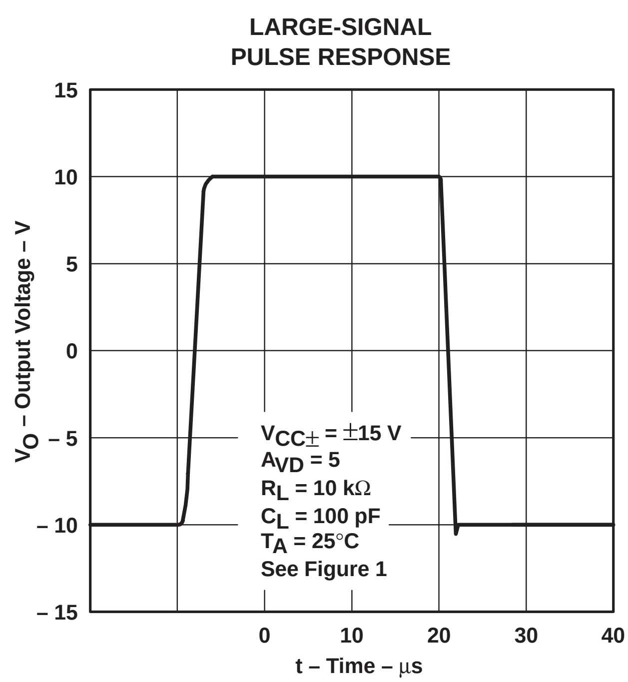


Figure 27

TYPICAL CHARACTERISTICS

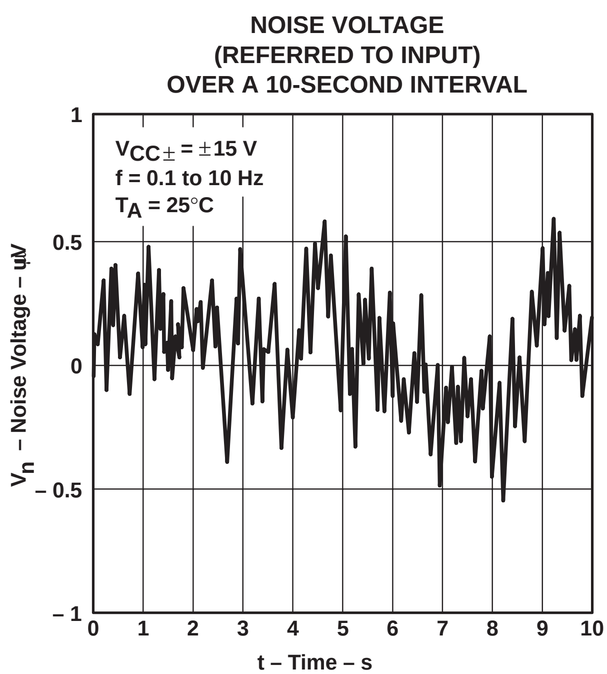


Figure 28

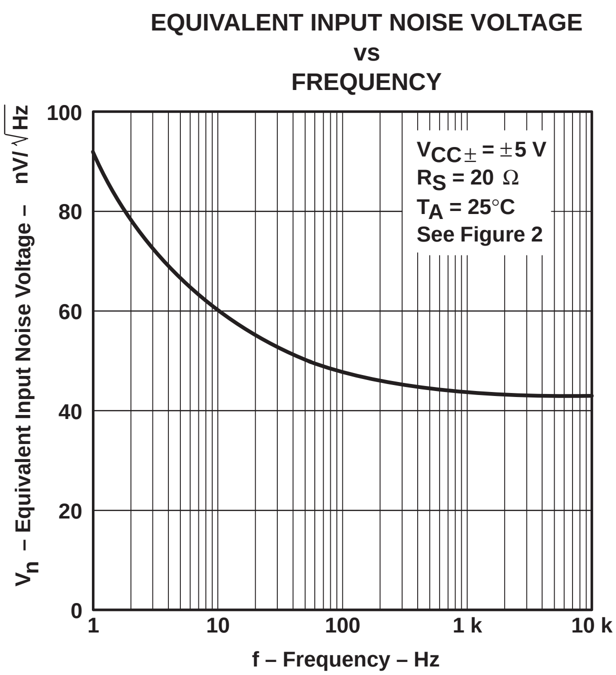


Figure 29

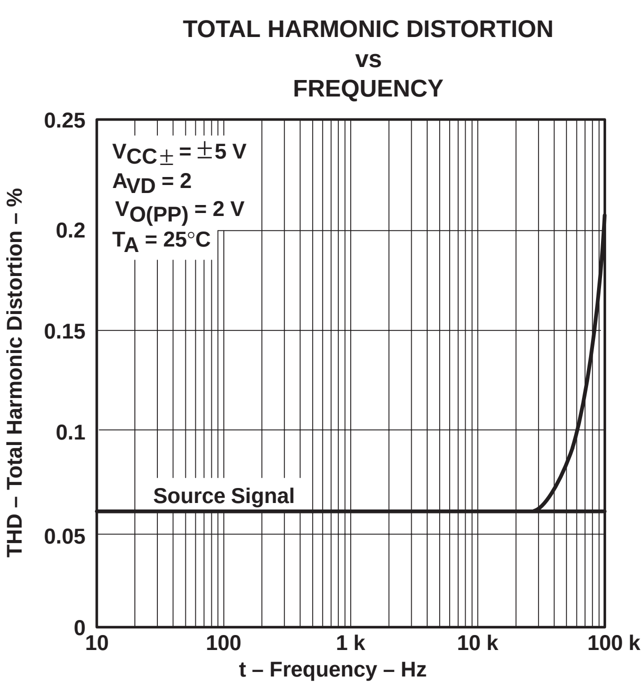


Figure 30

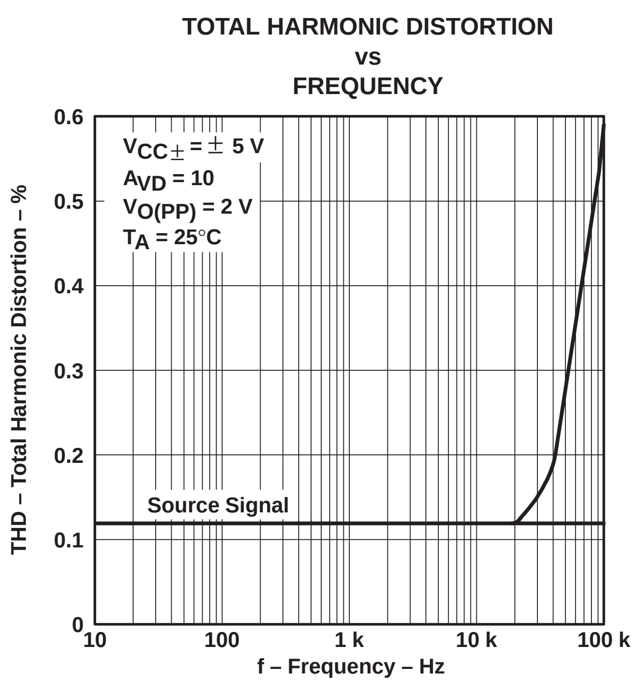


Figure 31

TYPICAL CHARACTERISTICS

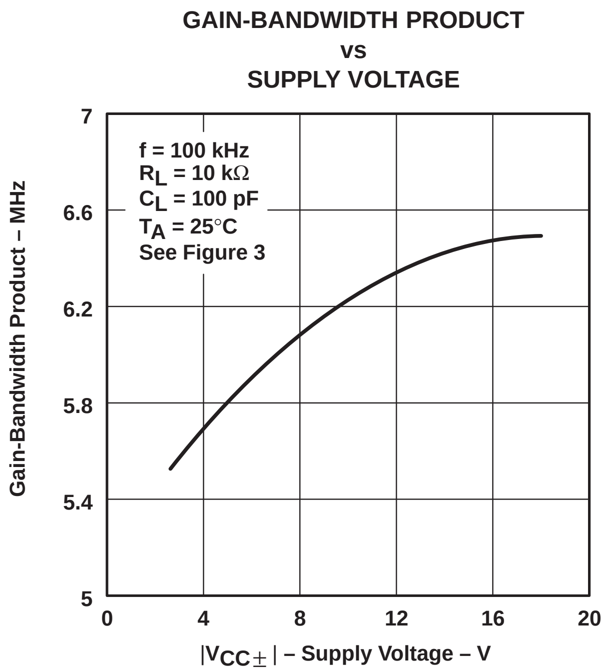


Figure 32

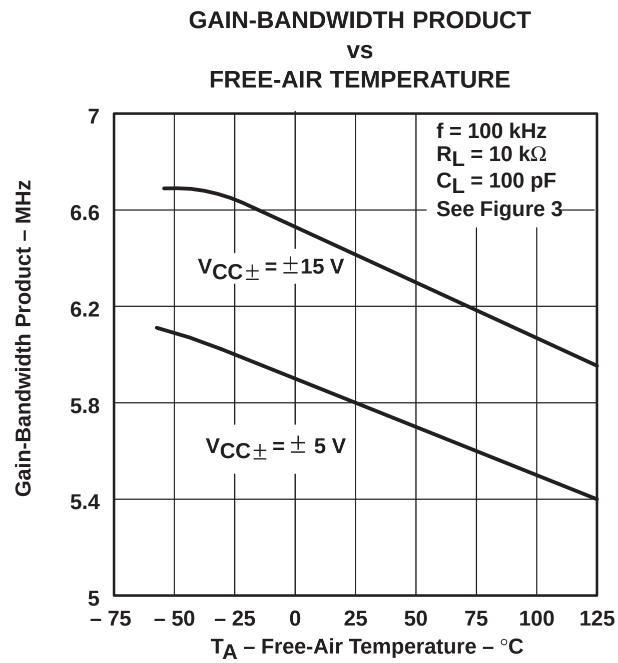


Figure 33

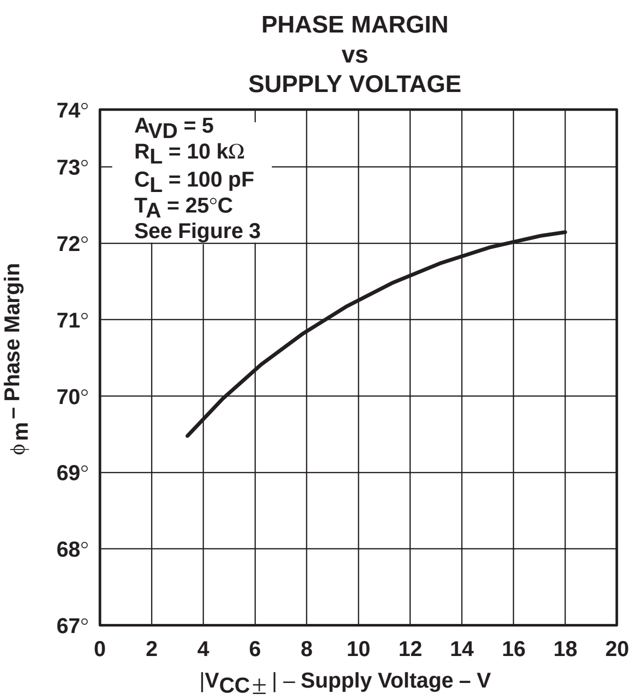


Figure 34

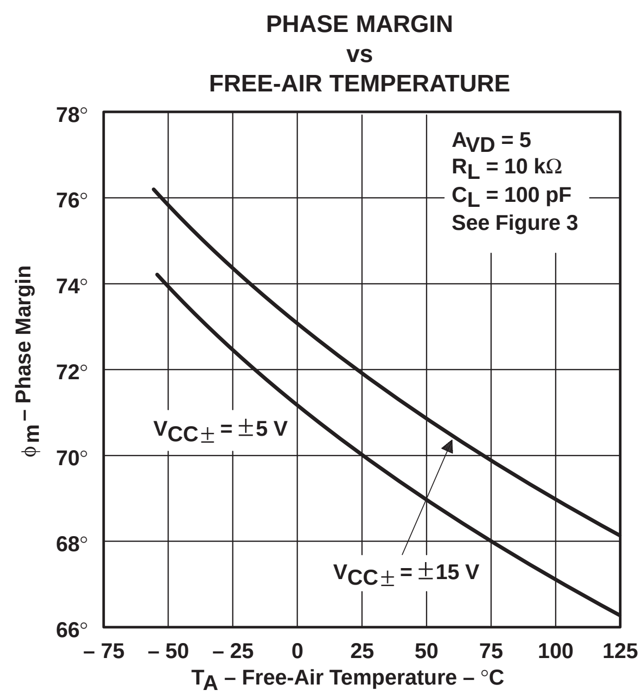


Figure 35

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 36 and Figure 37 were generated using the TLE2161 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Gain-bandwidth product
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

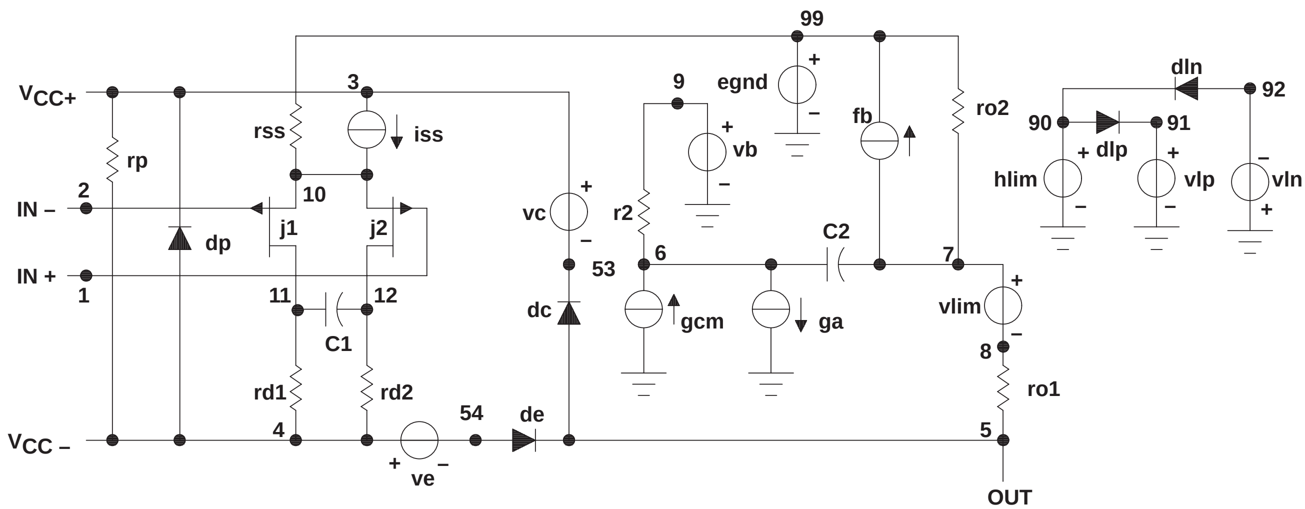


Figure 36. Boyle Macromodel

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, ”Macromodeling of Integrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

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APPLICATION INFORMATION

macromodel information (continued)

```
.subckt TLE2161 1 2 3 4 5
 c1    11  12  125.4E–14
 c2     6   7  5.000E–12
 dc     5  53  dx
 de    54  5d  x
 dlp   90  91  dx
 dln   92  90  dx
 dp     4   3  dx
 egnd  99   0  poly(2) (3,0) (4,0) 0 .5 .5
 fb     7  99  poly(5) vb vc ve vlp vln 0 4.085E6 –4E6 4E6 4E6 –4E6
 ga     6   0  11 12 201.1E–6
 gcm    0   6  10 99 3.576E–9
 iss    3  10  dc 45.00E–6
 hlim  90   0  vlim 1K
 j1    11   2  10 jx
 j2    12   1  10 jx
 r2     6   9  100.0E3
 rd1    4  11  4.973E3
 rd2    4  12  4.973E3
 ro1    8   5  280
 ro2    7  99  280
 rp     3   4  113.2E3
 rss   10  99  4.444E6
 vb     9   0  dc 0
 vc     3  53  dc 2
 ve    54   4  dc 2
 vlim   7   8  dc 0
 vlp   91   0  dc 50
 vln    0  92  dc 50
.model dx   D  (Is=800.0E–18)
.model jx PJF  (Is=1.000E–12 Beta=480E–6 Vto=–1)
.ends
```

Figure 37. Macromodel Subcircuit

APPLICATION INFORMATION

input characteristics

The TLE2161, TLE2161A and TLE2161B are specified with a minimum and a maximum input voltage that if exceeded at either input could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias-current requirements, the TLE2161, TLE2161A, and TLE2161B are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 38). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

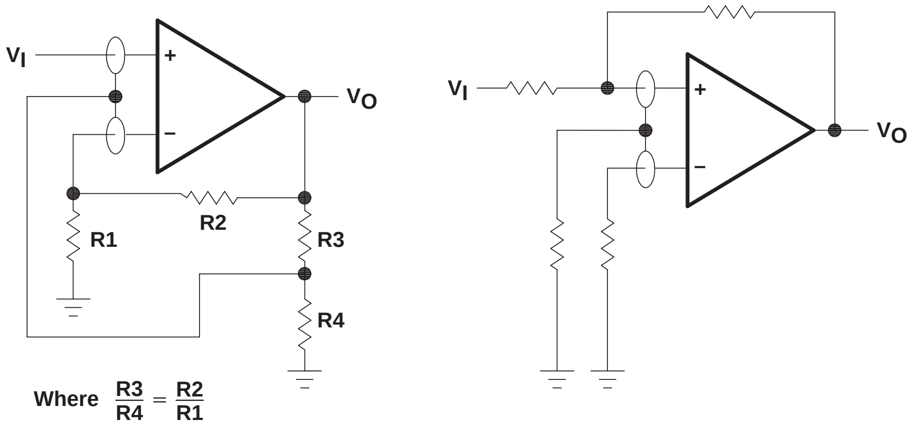

Figure 38. Use of Guard Rings

input offset voltage nulling

The TLE2161 series offers external null pins that can further reduce the input offset voltage. The circuit in Figure 39 can be connected as shown if the feature is desired. When external nulling is not needed, the null pins may be left disconnected.

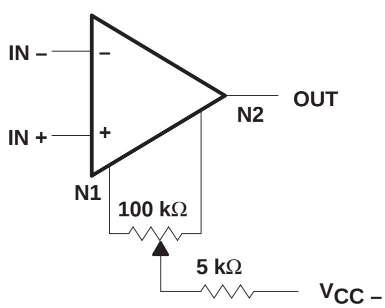

Figure 39. Input Offset Voltage Nulling

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9095801Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9095801QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9095802Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9095802QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9095803Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9095803QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLE2161ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161ACP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TLE2161AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161AIP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TLE2161AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLE2161AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLE2161BCP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TLE2161BIP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TLE2161BMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLE2161BMJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLE2161BMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLE2161BMP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TLE2161CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TLE2161ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLE2161IP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
TLE2161MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLE2161MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLE2161MP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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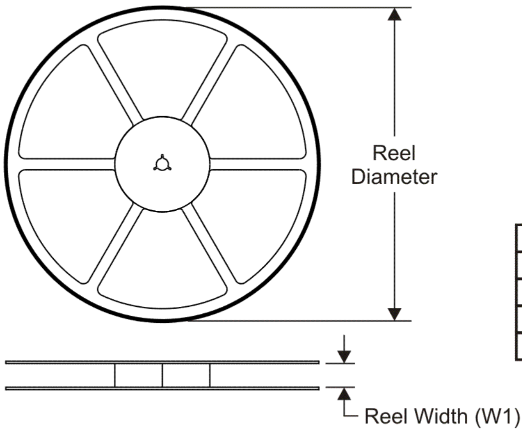
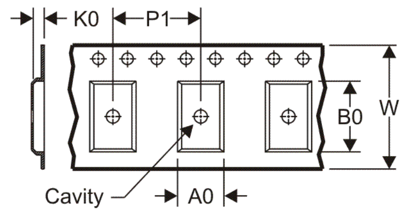
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

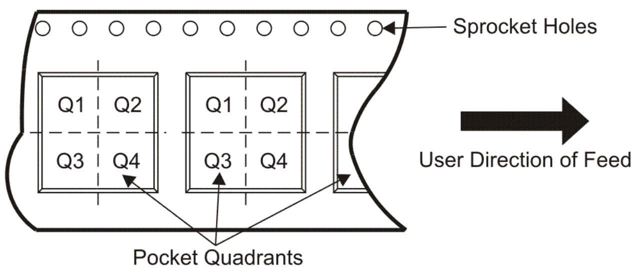


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

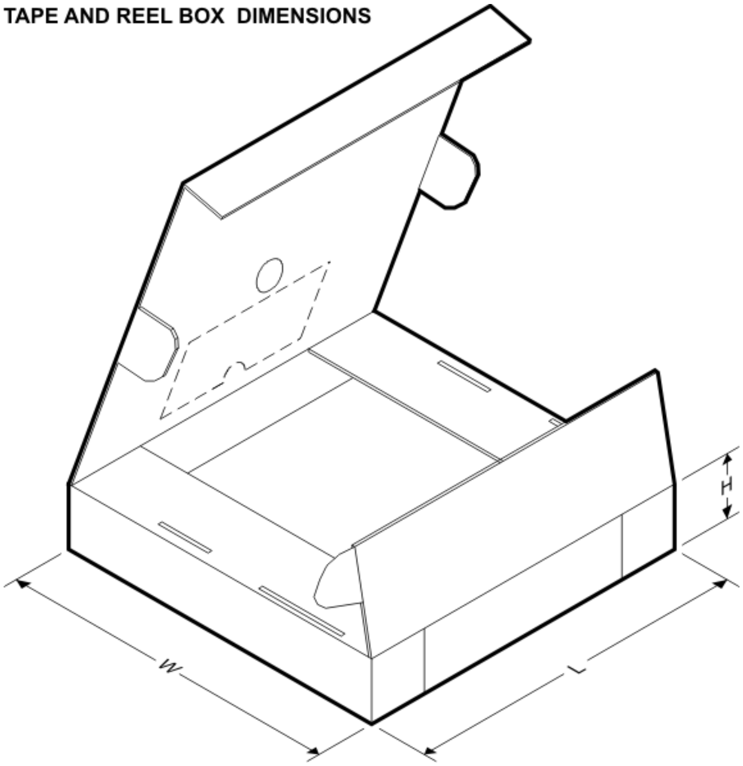
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLE2161AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2161AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLE2161IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLE2161AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLE2161AIDR	SOIC	D	8	2500	346.0	346.0	29.0
TLE2161IDR	SOIC	D	8	2500	346.0	346.0	29.0