# N-Channel 55-V (D-S), 175 °C MOSFET, Logic Level

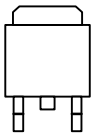
| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{(BR)DSS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
| 55 | 0.019 at $V_{GS}$ = 10 V | 40 |
| | 0.025 at $V_{GS}$ = 4.5 V | 35 |

## FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature

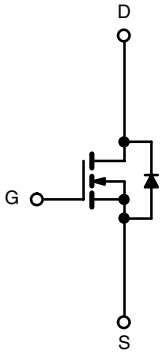
Available
RoHS* COMPLIANT

**TO-263**




Top View

DRAIN connected to TAB




N-Channel MOSFET

**Ordering Information:** SUM40N05-19L-E3 (Lead (Pb)-free)

| ABSOLUTE MAXIMUM RATINGS $T_C$ = 25 °C, unless otherwise noted | | | | |
|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Limit** | **Unit** |
| Drain-Source Voltage | | $V_{DS}$ | 55 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current ($T_J$ = 175 °C) | $T_C$ = 25 °C | $I_D$ | 40 | A |
| | $T_C$ = 100 °C | | 28 | |
| Pulsed Drain Current | | $I_{DM}$ | 80 | |
| Avalanche Current, Single Pulse | | $I_{AS}$ | 30 | |
| Avalanche Energy, Single Pulse | L = 0.1 mH | $E_{AS}$ | 45 | mJ |
| Power Dissipation | $T_C$ = 25 °C | $P_D$ | 65[a] | W |
| | $T_A$ = 25 °C[c] | | 3.1[b] | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | - 55 to 175 | °C |

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Limit** | **Unit** |
| Junction-to-Ambient | (PCB Mount)[b] | $R_{thJA}$ | 40 | °C/W |
| Junction-to-Case | | $R_{thJC}$ | 2.3 | |

Notes:
a. See SOA curve for voltage derating.
b. Surface Mounted on FR4 board, t ≤ 10 s.

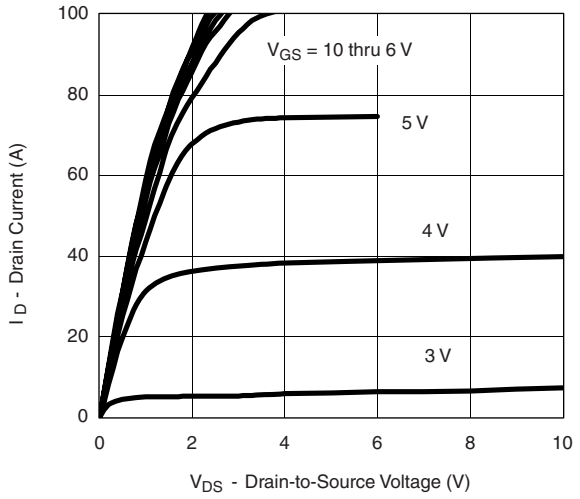
* Pb containing terminations are not RoHS compliant, exemptions may apply.

| **SPECIFICATIONS** $T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 55 | | | V |
| Gate-Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_{DS}$ = 250 µA | 1.0 | 2.0 | 3.0 | |
| Gate-Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 55 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $V_{DS}$ = 55 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | | | 50 | |
| | | $V_{DS}$ = 55 V, $V_{GS}$ = 0 V, $T_J$ = 175 °C | | | 250 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ = 5 V, $V_{GS}$ = 10 V | 40 | | | A |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 20 A | | 0.0155 | 0.019 | Ω |
| | | $V_{GS}$ = 10 V, $I_D$ = 20 A, $T_J$ = 125 °C | | | 0.033 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 20 A, $T_J$ = 175 °C | | | 0.040 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 15 A | | 0.020 | 0.025 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 20 A | | 50 | | S |
| **Dynamic[b]** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1 MHz | | 885 | | pF |
| Output Capacitance | $C_{oss}$ | | | 185 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 80 | | |
| Total Gate Charge[c] | $Q_g$ | $V_{DS}$ = 25 V, $V_{GS}$ = 10 V, $I_D$ = 35 A | | 10.5 | 13 | nC |
| Gate-Source Charge[c] | $Q_{gs}$ | | | 4 | | |
| Gate-Drain Charge[c] | $Q_{gd}$ | | | 4.8 | | |
| Gate Resistance | $R_g$ | f = 1.0 MHz | | 5.0 | | Ω |
| Turn-On Delay Time[c] | $t_{d(on)}$ | $V_{DD}$ = 25 V, $R_L$ = 0.3 Ω<br>$I_D$ ≅ 35 A, $V_{GEN}$ = 10 V, $R_G$ = 2.5 Ω | | 5 | 8 | ns |
| Rise Time[c] | $t_r$ | | | 18 | 30 | |
| Turn-Off Delay Time[c] | $t_{d(off)}$ | | | 20 | 30 | |
| Fall Time[c] | $t_f$ | | | 100 | 150 | |
| **Source-Drain Diode Ratings and Characteristics** $T_C$ = 25 °C[b] | | | | | | |
| Continuous Current | $I_S$ | | | | 35 | A |
| Pulsed Current | $I_{SM}$ | | | | 80 | |
| Forward Voltage[a] | $V_{SD}$ | $I_F$ = 35 A, $V_{GS}$ = 0 V | | 1.0 | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 35 A, di/dt = 100 A/µs | | 25 | 40 | ns |
| Peak Reverse Recovery Current | $I_{RM(REC)}$ | | | 1.5 | 2.5 | A |
| Reverse Recovery Charge | $Q_{rr}$ | | | 0.019 | 0.05 | µC |

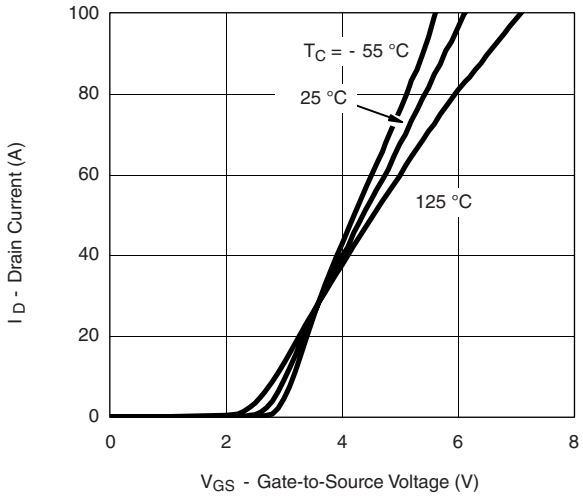
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

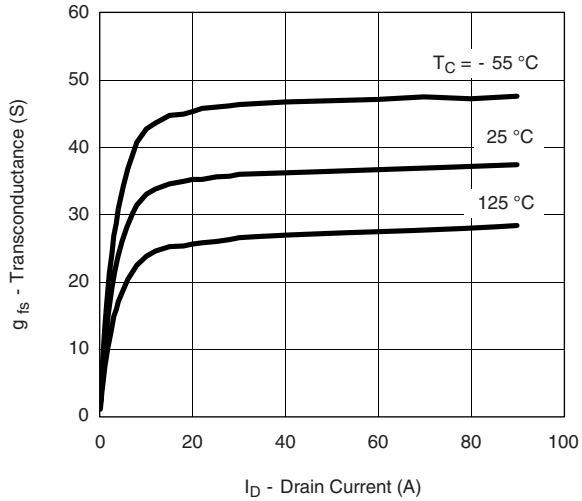
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



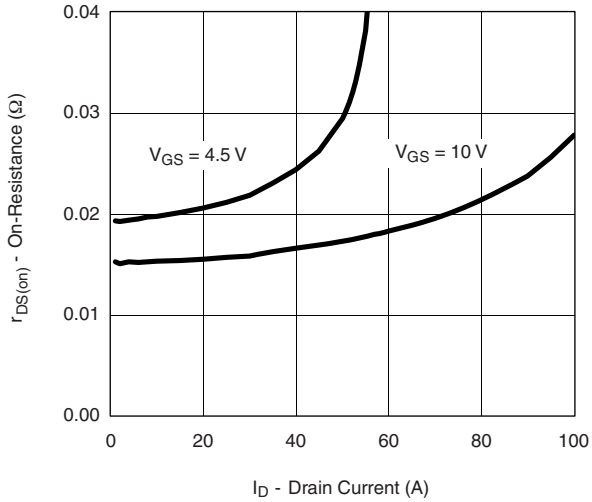

**Output Characteristics**



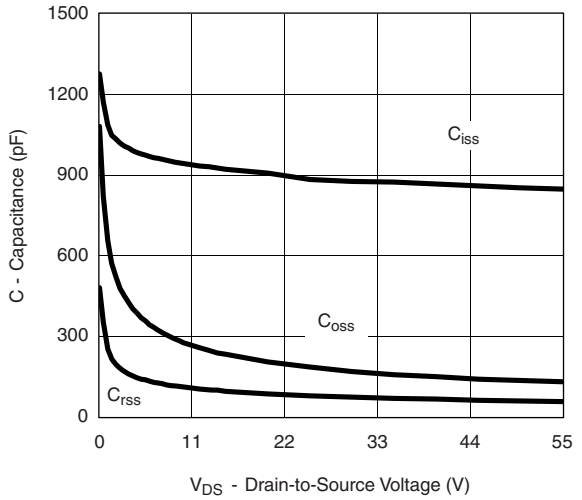

**Transfer Characteristics**



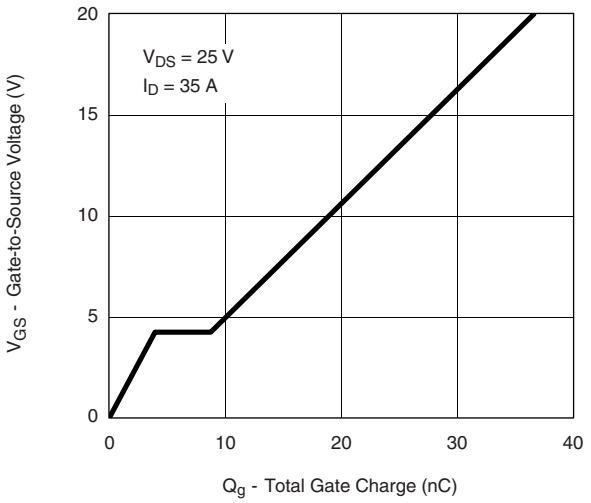

**Transconductance**




**On-Resistance vs. Drain Current**

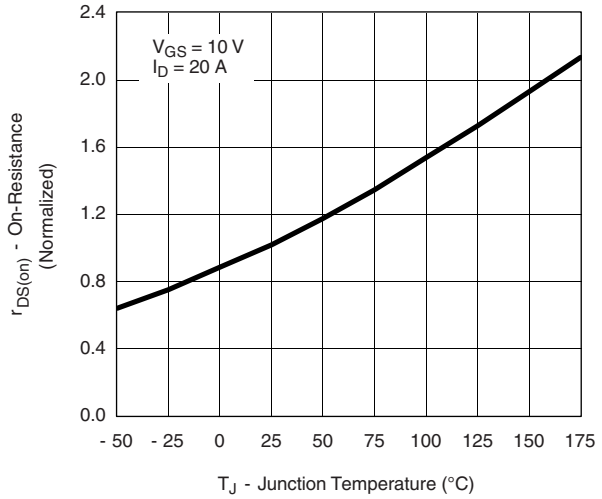



**Capacitance**

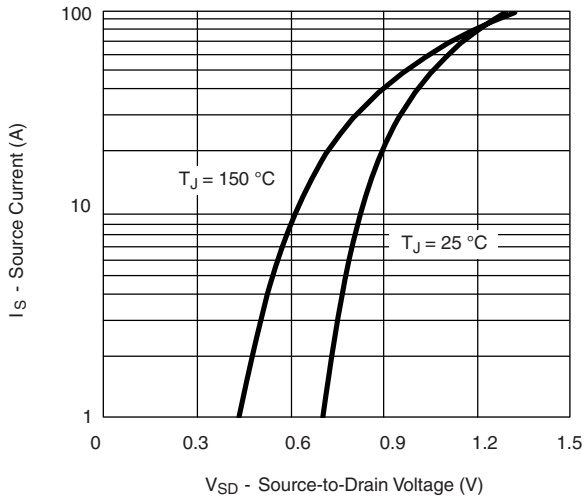



**Gate Charge**

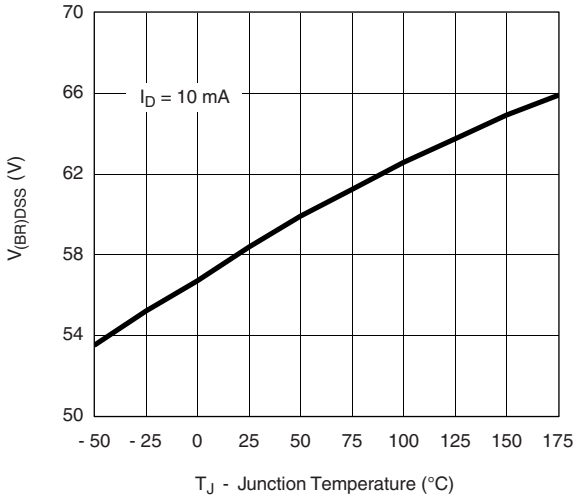
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted




**On-Resistance vs. Junction Temperature**

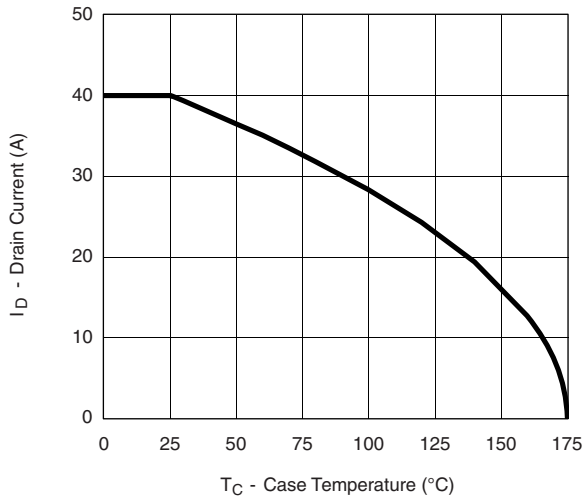



**Source-Drain Diode Forward Voltage**

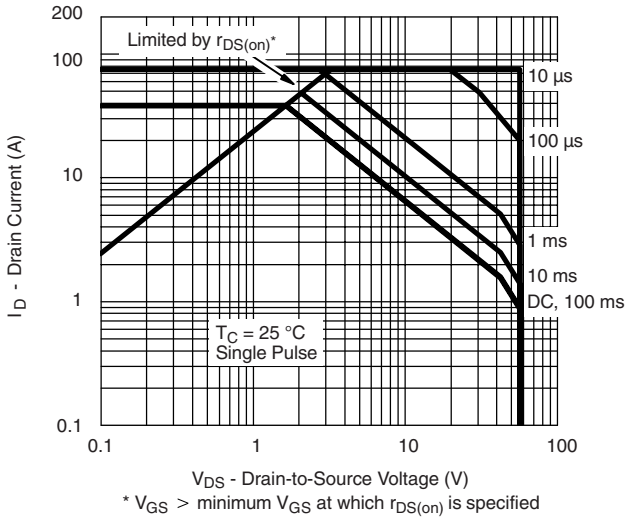



**Drain Source Breakdown vs. Junction Temperature**

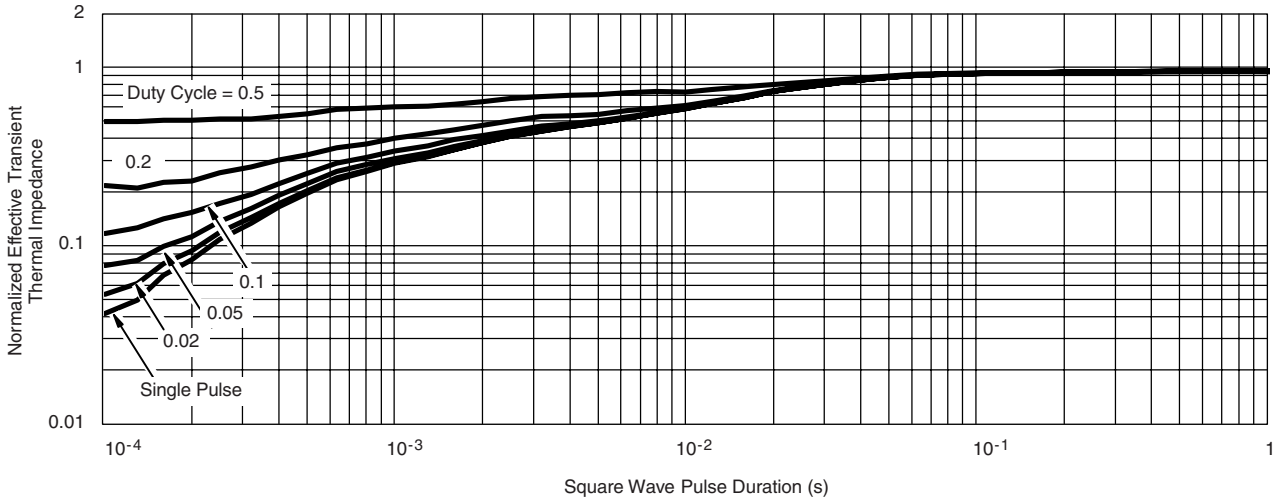
## THERMAL RATINGS




**Drain Current vs. Case Temperature**




**Safe Operating Area**




**Normalized Thermal Transient Impedance, Junction-to-Case**

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